Rev. Roum. Sci. Techn.– Électrotechn. et Énerg.
Vol. **63**, *2*, pp. 196–201, Bucarest, 2018

DESIGN OF NEW SYMMETRICAL NINE LEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES

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Key words: Multilevel inverter (MLI), Symmetric, Nine level, Total harmonic distortion (THD), Switching angle.

Multilevel inverter plays an important role in the field of modern power electronics. The objective of this paper is to design and simulate the modified symmetric multilevel inverter topology with reduced number of switches. The proposed inverter topology able to synthesize nine level output voltage during symmetric operation using four dc voltage sources and eight main switches. The different methods of calculating the switching angles were discussed in this paper. The MATLAB/Simulink software is used to simulate the proposed inverter. The performance of the proposed nine level inverter is analysed and the corresponding simulation and hardware results are presented in this paper. The experimental results justify the simulated response and the practical feasibility of the proposed nine level inverter topology for use in the field.

1. INTRODUCTION

The term "multilevel inverter" was first proposed in 1975 [1]. It plays a significant role in the field of power electronics and widely being used for many industrial and commercial applications. It uses a series of power semiconductor switches with several dc voltage sources. The staircase output voltage of the multilevel inverter is synthesized from several low or medium voltage dc sources. The dc voltage sources may be renewable energy resources, capacitors or batteries. The multilevel inverter have many advantages, such as, lower harmonic distortion, high power quality, lesser common mode voltage, minimum switching losses, minimum electromagnetic interference, better control, low switching losses, lower switching frequency, high voltage capability and reduces the stress of the switching devices [2, 3]. The most popular topologies of multilevel inverters includes diode-clamped multilevel inverter (DCMLI), flying capacitor multilevel inverter (FCMLI) and cascaded H-bridge multilevel inverter (CHMLI) [4–10].

In diode-clamped multilevel inverters, diodes are used as a clamping devices. The *n*-level diode-clamped multilevel inverters requires *n*–1 switching pairs and *n*–1 capacitors for clamping dc voltage [4, 5]. The switches are operate at low switching frequency. The main advantage is that the diode transfers very limited amount of voltage and thereby reduces the stress on the switching devices. However, it requires more number of clamping diodes to achieve higher level of output voltage and hence increases the cost and size. The capacitor clamped multilevel inverter uses capacitors instead of clamping diodes which controls both the real and reactive power flow. The large number of clamping capacitors helps to ride through short duration outages and deep voltage sags [6, 7]. The major drawbacks includes need of large number of storage capacitors, pre-charging of capacitors, high switching losses, poor efficiency, more expensive and bulky. The cascade H-bridge multilevel inverter consists of full H-bridges with independent dc voltage sources. As compared to DCMLI and FCMLI, cascaded H-bridge multilevel inverter requires less number of switching components to achieve same number of voltage levels [8]. The level of output voltage can be increased or decreased simply by adding or subtracting the dc sources. However, as the level of voltage increases, the number of active switches also increases according to 2(*N*–1) where *N* is the required voltage level [9, 10].

Many researchers has focused on developing new multilevel inverter topologies, novel pulse-width modulation (PWM) techniques and improved control techniques for various applications. A modified cascaded multilevel inverter is proposed in [11]. This inverter consists of active input rectifier and H-bridge inverter. This inverter have the capability to control the input current and output voltage during the motoring and regenerative mode of operation. An asymmetric type multilevel inverter topology is proposed in [12]. In this, each unit consists of four unequal dc voltage sources and 10 switches to produce 13 level output voltage. A new H-bridge based multilevel inverter is proposed in [13]. This inverter topology uses 2 dc voltage sources and 6 switches to produce seven level output voltage during symmetric operation. Even though many inverter topologies have been introduced, still there is a need to optimize the switch count and reduce the total harmonic distortion to improve the power transfer quality.

This paper aims to establish a new symmetrical multilevel inverter topology that requires eight switches for arriving nine level output waveform.

2. PROPOSED INVERTER TOPOLOGY

The circuit diagram of the proposed nine level inverter is shown in Fig. 1.

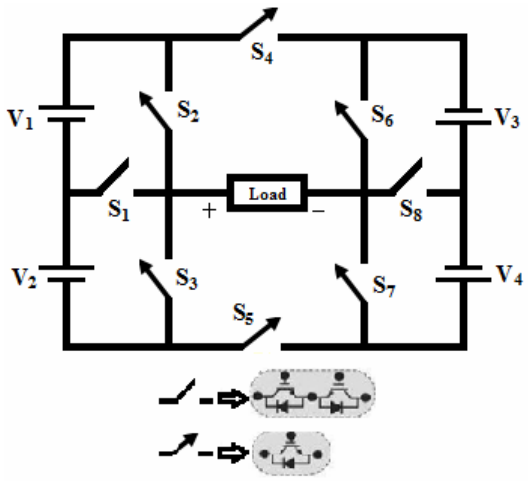

Fig. 1 – Proposed 9 level inverter.

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This inverter topology consists of eight switches and four dc voltage sources to produce the nine level output voltage waveform. The proposed inverter topology inherits the advantage of using isolated series connected dc voltage sources either from a dc link or any renewable energy sources. The switches S_1 and S_8 are bidirectional and the other switches are unidirectional. Table 1 explains the switching states of different modes of operation of the proposed inverter topology for producing the positive/negative cycles of the output voltage across the load.

The different operating modes of the proposed inverter topology are shown in Fig. 2. The mode-1 operation is shown in Fig. 2a. During this mode of operation, the switches S_3, S_5 and S_8 are ON and the other switches were OFF and hence the level-1 voltage is obtained across the load. In mode-2, the switches S_3, S_5 and S_6 are ON and the other switches were OFF and hence the level-2 voltage is obtained across the load as shown in Fig. 2b. During mode-3 operation, the switches S_1, S_5 and S_6 are ON and the other switches were OFF and hence the level-3 voltage is obtained across the load as shown in Fig. 2c. During mode-4 operation, the level-4 voltage is obtained across the load with the switches S_2, S_5 and S_6 are ON and the other switches were OFF as shown in Fig. 2d. During mde-5, the zero voltage is obtained across the load as shown in Fig. 2e. In this mode, the switches S_2, S_4 and S_6 are ON. The mode-1 to mode-4 operation are called as positive mode of operation where the voltage obtained across the load is positive. During negative mode of operation from mode-6 to mode-9, the negative voltage level is obtained across the load terminals. The negative modes of operation are shown in Fig. 2f – Fig. 2i. From Table 1, it is observed that only three switches were ON to achieve any required output voltage levels. This shows that the stress on the switches has been considerably reduced and minimizes the switching losses. In the proposed topology, the maximum voltage stress on switches S_1 and S_8 is equal to V_{dc}. For switches S_2, S_3, S_6 and S_7, the maximum voltage stress is equal to 2 V_{dc}. Similarly, for switches S_4 and S_5, the maximum voltage stress is equal to 4 V_{dc}. Therefore, the total maximum voltage stress on switches is equal to 18 V_{dc}.

Figure 3 shows the comparison of the maximum number of ON state switches required to achieve the nine level output voltage for the proposed and other symmetric multilevel inverter topologies.

Table 1

Switching states

S. No	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output
1	0	1	0	0	1	1	0	0	$V_1+V_2+V_3+V_4$
2	1	0	0	0	1	1	0	0	$V_2+V_3+V_4$
3	0	0	1	0	1	1	0	0	V_3+V_4
4	0	0	1	0	1	0	0	1	V_4
5	0	0	1	0	1	0	1	0	0
6	0	1	0	1	0	1	0	0	
7	1	0	0	1	0	1	0	0	$-V_1$
8	0	0	1	1	0	1	0	0	$-(V_1+V_2)$
9	0	0	1	1	0	0	0	1	$-(V_1+V_2+V_3)$
10	0	0	1	1	0	0	1	0	$-(V_1+V_2+V_3+V_4)$

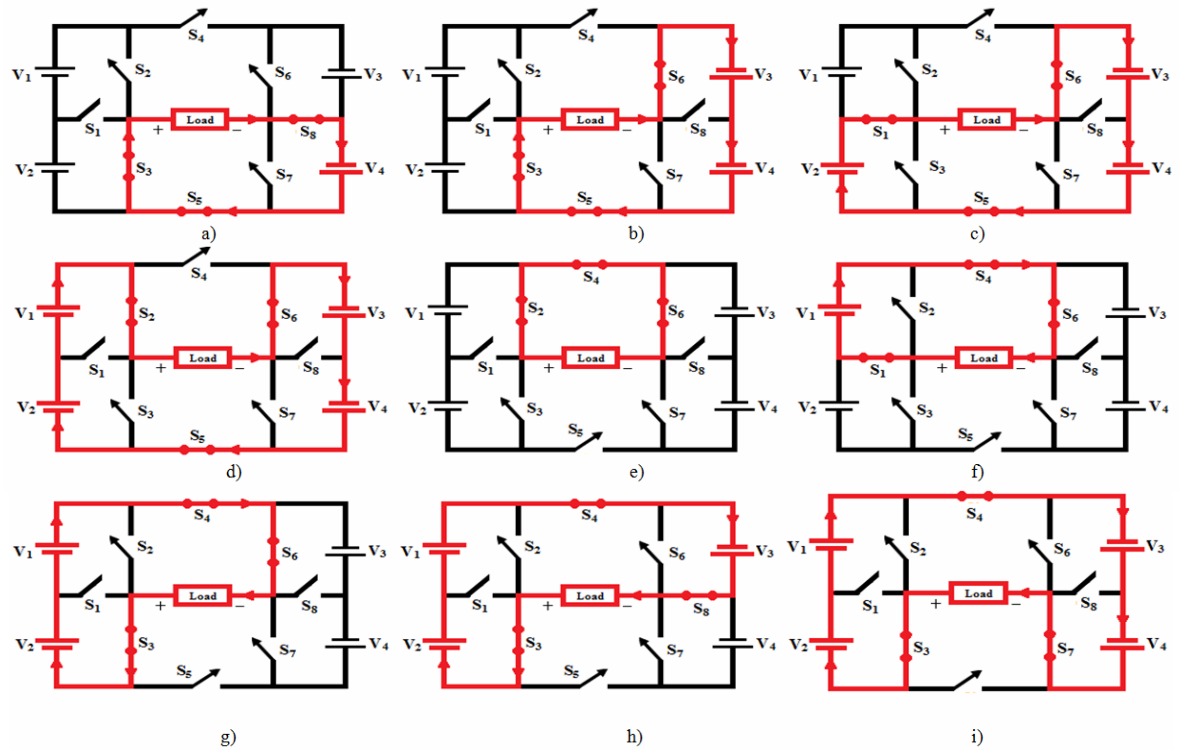


Fig. 2 – Modes of operation: a) Mode 1; b) Mode 2; c) Mode 3; d) Mode 4; e) Mode 0; f) Mode 5; g) Mode 6; h) Mode 7; i) Mode 8.

The comparison of the output voltage levels with the number of dc voltage sources and the number of switches for different topologies of symmetrical multilevel inverter are given in Table 2.

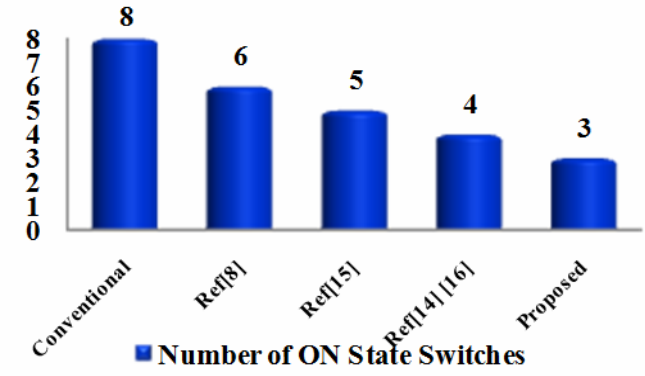


Fig. 3 – Proposed multilevel inverter.

Table 2

Comparison of different multilevel inverters

Inverter	Number of dc sources (N_{dc})	Number of switches (N_S)	Number of level (N)	Ratio (N_S / N)
Cascaded H-bridge inverter	4	16	9	1.78
Ref. [8], [12], [14],[15]	4	10	9	1.11
Ref. [10]	4	11	9	1.22
Ref. [13], [16]	4	12	9	1.33
Ref. [17]	4	20	9	2.22
Proposed inverter	4	8	9	0.88

Table 2 shows that the ratio of the number of switches to the number of output levels for the proposed inverter topology is 0.88 which is less compared with other inverter topologies. Therefore, it is clear that the proposed multilevel inverter uses minimum number of switches to achieve nine level output voltage.

3. SWITCHING ANGLE CALCULATION

Switching angles has an important role in the reduction of total harmonic distortion (THD). Generally, the switching pulses for the MLIs were obtained using the carrier based PWM techniques. In carrier based PWM technique, the reference signal is compared with the carrier signals and the switching pulses were generated. A PWM control scheme is proposed in [18], which utilizes three reference signals and a triangular carrier signal, for a single phase seven level inverter for grid connected photovoltaic applications. A generalised PWM sub harmonic method is proposed in [19], to control the multilevel voltage source inverters (VSI). A selective harmonic mitigation pulse-width modulation (SHM-PWM) technique based on multilevel waveforms is presented in [20]. It enables the required control of power flow in a cascaded H-bridge inverter and fully utilizes the waveform degrees of freedom. A modified SHM-PWM technique is proposed in [21], which employs variable dc link voltages as a degree of freedom. In [22], a series space vector modulation (SVM) method has been proposed for cascaded H-bridge multilevel inverters. In this paper, a non-carrier based (i.e., carrier less) PWM techniques is adopted to generate switching pulses for the proposed inverter. Here, the switching angles were calculated directly using the formula.

The switching angles corresponding to the period 0 to $\pi/2$ are called as main switching angles. An n level inverter has $(n–1)/2$ main switching angles. It is enough to determine the $(n–1)/2$ main switching angles and the other switching angles are obtained from the main switching angles using the following relations [23]:

1. For period 0 to $\pi/2$
   $= \theta_1, \theta_2, \ldots, \theta_{(n-1)/2}$.

2. For period $\pi/2$ to π
   $= \theta_{(n+1)/2}. \ldots, \theta_{(n-1)}. = (\pi-\theta_{(n-1)/2}),. \ldots,(\pi-\theta_1)$.

3. For period π to $3\pi/2$
   $= \theta_n, \ldots, \theta_{3(n-1)/2} = (\pi+\theta_1),. \ldots,(\pi+\theta_{(n-1)/2})$.

4. For period $3\pi/2$ to 2π
   $= \theta_{(3n-1)/2}, \ldots, \theta_{2(n-1)}$
   $= (2\pi - \theta_{(n-1)/2}),. \ldots,(2\pi-\theta_1)$.

There are totally $2(n–1)$ switching angles has to be determined for n level inverter [23]. The different methods of calculating switching angles are given below:

Method 1. The switching angles are distributed averagely over the range 0–π and are determined by,

$$\theta_j = j\frac{180^0}{n} \text{ where } j = 1,2,\ldots,\left(\frac{n-1}{2}\right). \quad (1)$$

Method 2. The main switching angles are determined by,

$$\theta_j = j\frac{180^0}{n+1} \text{ where } j = 1,2,\ldots,\left(\frac{n-1}{2}\right). \quad (2)$$

Method 3. The gaps between the positive half-cycle and the negative half-cycle were reduced by using the following formula,

$$\theta_j = \frac{1}{2}\sin^{-1}\left(\frac{2j-1}{n-1}\right) \text{ where } j = 1,2,\ldots,\left(\frac{n-1}{2}\right). \quad (3)$$

Method 4. It gives better output voltage waveform. The main switching angles are determined by the following formula,

$$\theta_j = \sin^{-1}\left(\frac{2j-1}{n-1}\right) \text{ where } j = 1,2,\ldots,\left(\frac{n-1}{2}\right). \quad (4)$$

The switching angles of n-level inverter is shown in Fig. 4. The nine level output voltage obtained during positive and negative cycles are shown in Fig. 5.

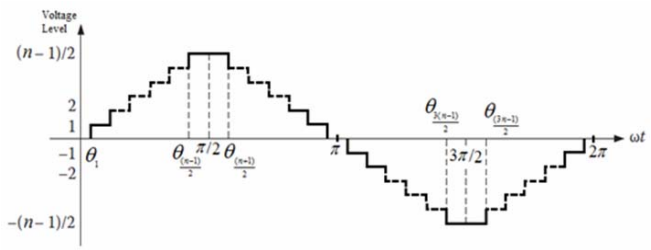
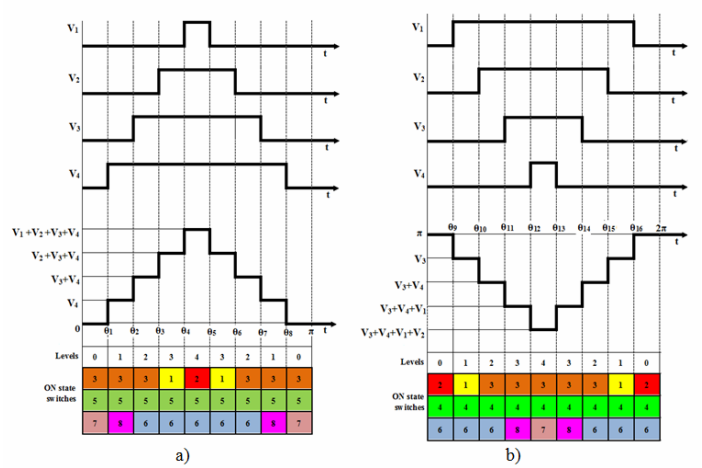
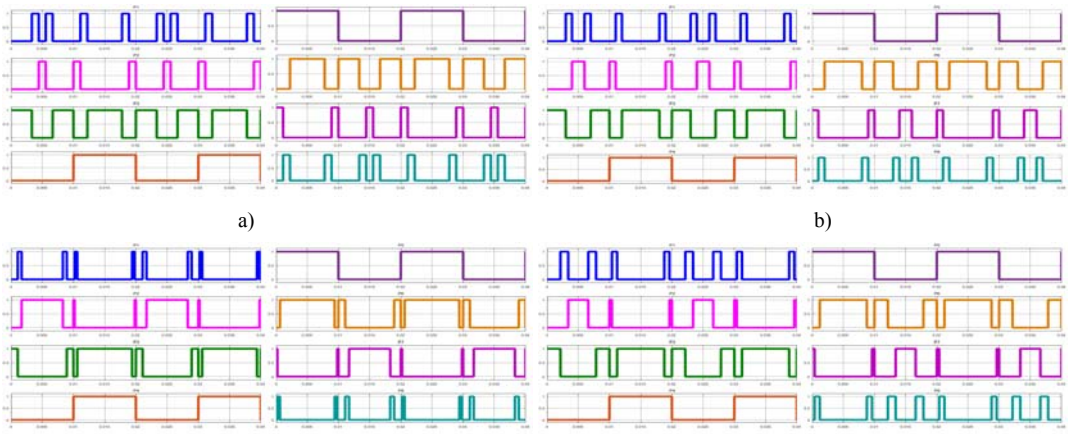


Fig. 4 – Output voltage waveform with switching angles for a *n* level inverter.



a) b)

Fig. 5 – Nine level output voltage: a) positive cycle; b) negative cycle.



a) b)

c) d)

Fig. 6 – Switching pulses: a) Method 1; b) Method 2; c) Method 3; d) Method 4.

The switching pulses generated using the different methods are shown in Fig. 6. For the proposed multilevel inverter, there are four main switching angles and are determined using the above mentioned methods are given in Table 3.

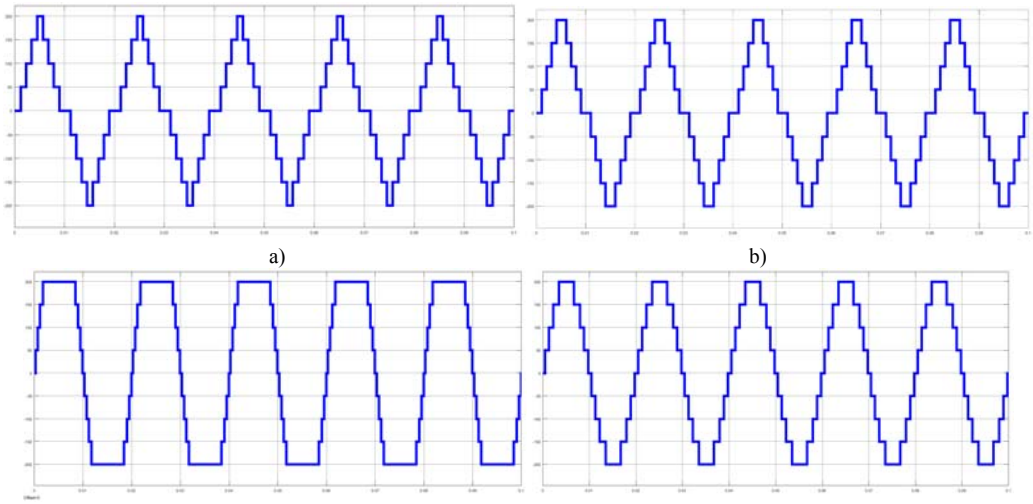
Table 3

Switching angles

Angle	Main switching angles (in degree)			
	Method 1	**Method 2**	**Method 3**	**Method 4**
θ_1	20	18	3.5904	7.1808
θ_2	40	36	11.0122	22.0243
θ_3	60	54	19.3411	38.6822
θ_4	80	72	30.5225	61.045

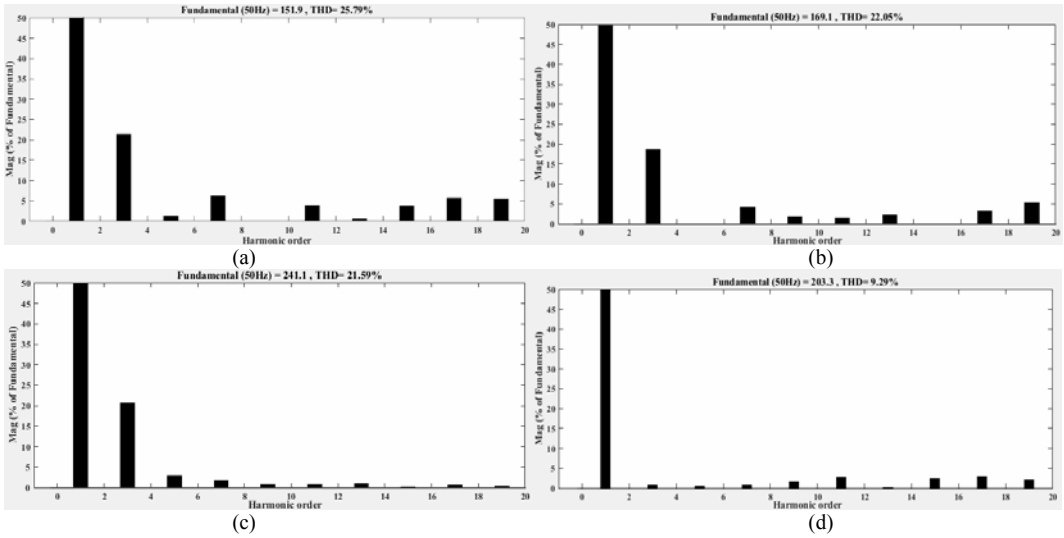
4. RESULTS AND DISCUSSION

The MATLAB/Simulink simulation results and hardware results of the proposed symmetrical nine level inverter are presented in this section. The proposed inverter consists of four dc voltage sources and eight main switches. The magnitude of all dc voltage sources are equal *i.e.*, $V_1 = V_2 = V_3 = V_4 = V_{dc} = 50$ V. The maximum voltage obtained is equal to 200 V (*i.e.*, $V_1 + V_2 + V_3 + V_4$). A series RL load with magnitudes $R = 50\ \Omega$ and $L = 35$ mH are considered as load parameters. The nine level output voltage obtained for different switching methods are shown in Fig. 7. The fast Fourier transform (FFT) analysis of the output voltage waveform for different switching method are shown in Fig. 8.



a) b) c) d)

Fig. 7 – Nine level output voltage waveform: a) Method 1; b) Mehtod 2; c) Method 3; d) Method 4.



(a) (b) (c) (d)

Fig. 8 – FFT analysis of the nine level output voltage waveform: a) Method 1; b) Mehtod 2; c) Method 3; d) Method 4

Table 4

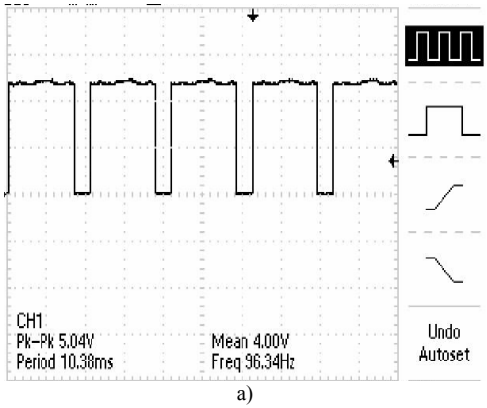
Comparison of fundamental output voltage and THD

Method	Fundamental output voltage (V)	THD (%)
Method 1	151.9	25.79
Method 2	169.1	22.05
Method 3	241.1	21.59
Method 4	203.3	**9.29**

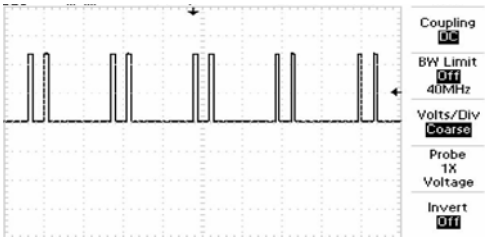
The simulation result shows that the harmonic content of the nine level output voltage waveform for the switching method – 4 is less as 9.29 % when compared with the other methods. The comparison of the fundamental output voltage and % THD are given in Table 4. The measured input and output powers are about 520 W and 478.92 W, respectively with the loss of 41.08 W. Therefore, the efficiency of the proposed inverter is about 92.1 %.

This hardware setup of the proposed nine level inverter is shown in Fig. 9. The gate pulses are generated using PIC16F87XA. The operating frequency of PIC16F87XA is 20 MHz. The IGBT FGW40N120HD with a 1200 V/40 A capacity is used as switching device in the hardware setup. The output of the inverter is observed using oscilloscope.

Fig. 9 – Hardware setup.



a)



b)

Fig. 10 – Switching pulses: a) Switch 3; b) Switch 8.

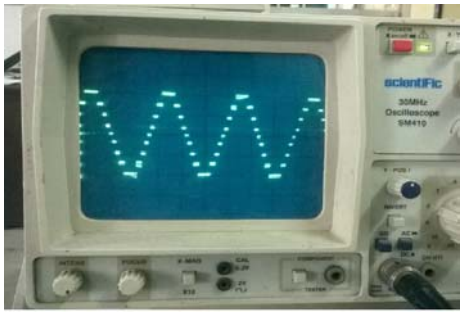


Fig. 11 – Hardware output of nine level voltage waveform.

The sample switching pulses obtained from the hardware setup is shown in Fig. 10. The nine level output voltage waveform obtained across the load is shown in Fig. 11. The experimental results justify the simulated response and the practical feasibility of the proposed nine level inverter topology for use in the field.

5. CONCLUSIONS

A new symmetric type nine level inverter with minimum number of switches has been proposed in this paper. The main advantage of this inverter topology is it uses only four dc voltage sources of equal magnitude and eight main switches to achieve nine level output voltage as compared with other conventional topologies. The four different methods used to calculate the switching angles are presented and the simulation results are compared in this paper. The maximum obtained voltage is equal to the sum of the magnitude of the individual voltage. The simulation result shows that the switching angles obtained by method 4 achieves less THD compared with other methods. The major advantage of the proposed multilevel inverter is it uses minimum number of switches and hence the cost and the size of the inverter is reduced.

Received on April 1, 2017

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