CMOS LOGARITHMIC CURVATURE-CORRECTED VOLTAGE REFERENCE BY USING A MULTIPLE DIFFERENTIAL STRUCTURE

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Key words: **Temperature behavior, Superior-order curvature-correction technique, Voltage references.**

A new superior-order curvature-corrected voltage reference will be presented. In order to improve the temperature behavior of the circuit, a double differential structure will be used, implementing both the linear and the superior-order curvature corrections. The superior-order curvature-correction will be implemented by taking the difference between two gate-source voltages of subthreshold-operated MOS transistors, biased at drain currents having different temperature dependencies: PTAT (ProporTional with Absolute Temperature) and $PTAT^2$. The SPICE simulations confirm the theoretical estimated results, showing a temperature coefficient under 9.4 ppm/K for an extended input range 173 K < T < 423 K and for a supply voltage of 2.5 V and a current consumption of about 1 μA.

1. **INTRODUCTION**

Very important stages in applications such as A/D and D/A converters, data acquisition systems, memories or smart sensors, voltage reference circuits and theirs temperature behavior are intensively studied in the last decade and many researches have been developed for improving them.

There were developed a lot of curvature-correction techniques [1–6] for improving the temperature behavior of the voltage reference: exponential, optimal, polynomial and generalized polynomial corrections or the compensation based on an adaptive temperature. All these previous techniques present the important disadvantages of an important value of the temperature coefficient, a relatively large value of the minimal supply voltage or an important current consumption.

The new proposed realization of the CMOS voltage reference is a low-voltage low-power circuit designed for an extreme temperature behavior, using a gate-source voltage of a subthreshold-operated MOS transistor as a zero-order compensated voltage reference. The linear decreasing with temperature term from $V_{GS}(T)$ will be compensated using a complementary $CTAT$ voltage, obtained using an original approach based exclusively on MOS active devices, while the

logarithmic dependent on temperature term from $V_{GS}(T)$ will be cancel out by a proper difference between two gate-source voltages of MOS transistors biased at drain currents with different temperature dependencies. The simulated results show a very good temperature behavior of the circuit with respect to the previous implementations of a superior-order curvature-corrected voltage references.

2. **THEORETICAL ANALYSIS**

2.1. THE BLOCK DIAGRAM OF THE VOLTAGE REFERENCE CIRCUIT

The block diagram of the original proposed voltage reference with superior-order curvature-correction is presented in Fig. 1, containing:

– A zero-order curvature-corrected voltage reference (ZVR);

– A double-differential structure (DDS), which represents the core of the circuit, implementing the linear and the superior-order curvature-corrections;

– An auxiliary current reference (ACR) for obtaining a PTAT current and a current approximately independent on temperature (in a first-order analysis);

– A current squarer (CSQ) for implementing a current with $PTAT^2$ dependence.

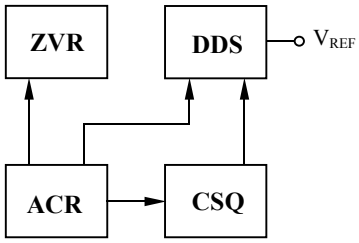

Fig. 1 – The block diagram of the superior-order curvature-corrected voltage reference.

2.2. THE ZERO-ORDER CURVATURE-CORRECTED VOLTAGE REFERENCE (ZVR)

The gate-source voltage of a MOS transistor working in weak inversion represents the simplest implementation in CMOS technology of a voltage generator with small negative temperature dependence [7]:

$$V_{GS}(T) = V_{FB} + E_{G0} + \frac{V_{GS}(T_0) - V_{FB} - E_{G0}}{T_0} T + \frac{nkT}{q}(\alpha + \gamma - 2)\ln\frac{T}{T_0}, \qquad (1)$$

where E_{G0} is the silicon bandgap energy, V_{FB} and γ are not dependent on temperature, T_0 is the reference temperature and α models the temperature dependence of the drain current that biases the MOS transistor, $I_D(T) = ct \cdot T^{\alpha}$. The first term is a constant term, the second one is a linear term, which will be compensated by a complementary linear dependent on temperature voltage and the last term models the nonlinearity of the gate-source voltage temperature dependence. This term will be compensated by a suitable logarithmic dependent on temperature voltage, also added with $V_{GS}(T)$.

2.3. LOW-POWER OPERATION BANDGAP REFERENCE USING DTMOST

A very important trend in designing low-power analog and/or digital circuits are a continuous decreasing of the supply voltage. When correctly designed, bandgap reference circuits give an output voltage that is somewhat higher than the material bandgap extrapolated to 0K. Typical bandgap references need at least an extra voltage of $100 - 300$ mV for proper operation, depending on technology. The minimum supply voltage for the typical bandgap circuit is then approximately:

$$V_{CC\,\min} = V_{REF} + 300 \text{ mV} \approx 1.5 \text{ V}. \tag{2}$$

With newer CMOS processes, the nominal supply voltage decreases. In 0.5 μm CMOS processes, the nominal supply voltage is 3.3 V; for 0.25 μm CMOS, it is 2.5 V and for 0.15 μm CMOS the supply voltage is 1.5 V and will continue to decrease with each newer process generation. In conclusion, for these processes, the traditional bandgap reference circuit cannot be used because of the too small value of the supply voltage. In order to obtain a proper operation of the classical bandgap reference at low supply voltages, there are some possible solutions:

– The utilization of a low-bandgap material (germanium) to realize low-bandgap diodes. It is very expensive and not available in standard CMOS processes;

– The utilization of a fraction of the voltage across the diodes, by resistive division. The disadvantage is a considerable area consumption because of the large value resistors, imposed by a low-power operation;

– The lowering of the equivalent material bandgap, using an electrostatic field, is used in this section.

On layout level, the DTMOST is a MOS transistor with an interconnected well and gate. Using diodes with a low apparent material bandgap (implemented with DTMOSTs) for replacing the classical MOS active device, the result will be a bandgap reference circuit with a lower output voltage and a lower required supply voltage.

2.4. THE DOUBLE-DIFFERENTIAL STRUCTURE (DDS)

The core of the superior-order curvature-corrected voltage reference is represented by the DDS block (Fig. 2), all MOS transistors working in weak inversion. Two important features could be achieved using this block: the linear and the superior-order curvature corrections.

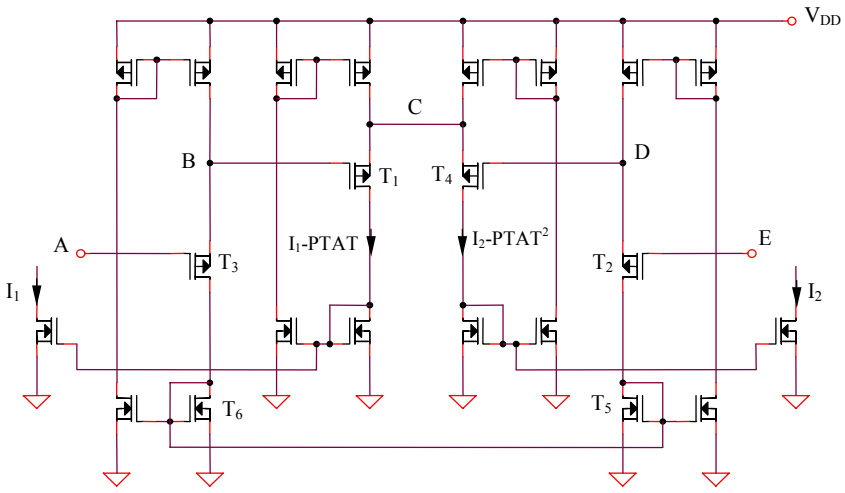

Fig. 2 – The double-differential structure.

2.4.1. THE LINEAR CURVATURE CORRECTION

The linear curvature correction technique is necessary for compensate the linear decreasing with temperature term from (1). This complementary term will be obtained by using the difference between two gate-source voltages (V_{GS2} and V_{GS3} from Fig. 2, respectively). The implementation of a PTAT voltage generator (T_2, T_3, T_5 and T_6) presents the important advantages of a strongly reduced silicon area and of an improved accuracy obtained by replacing all the resistors from the circuit by MOS active devices. The linear curvature-correction voltage is represented by $V_{ED}(T)+V_{BA}(T)$, having the following expression:

$$V_{LIN}(T)=\left|V_{GS3}(T)\right|-\left|V_{GS2}(T)\right|. \tag{3}$$

The linear correction voltage will be:

$$V_{LIN}(T)=\frac{nkT}{q}\ln\left[\frac{(W/L)_2(W/L)_6}{(W/L)_3(W/L)_5}\right]. \tag{4}$$

Choosing $(W/L)_2(W/L)_6 > (W/L)_3(W/L)_5$, the previous voltage will have a PTAT variation, which will compensate the linear decreasing with temperature of $V_{GS}(T)$ from (1).

2.4.2. THE SUPERIOR-ORDER CURVATURE-CORRECTION TECHNIQUE

The goal of this technique is to remove the logarithmic dependent on temperature term from (1) by inserting a circuit able to compute a voltage complementary to this term. The original method for implemented the superior-order curvature-correction is to consider the difference of gate-source voltages for MOS transistors biased at drain currents with different temperature dependencies. The superior-order correction voltages could be expressed as:

$$V_{SUP}(T) = V_{DB}(T) = \left|V_{GS1}(T)\right| - \left|V_{GS4}(T)\right|. \tag{5}$$

Transistor T_1 is biased at a PTAT current, so its gate-source voltage will have the following temperature dependence:

$$\left|V_{GS1}(T)\right| = V_{FB} + E_{G0} + \frac{V_{GS}(T_0) - V_{FB} - E_{G0}}{T_0} T + \frac{nkT}{q}(\gamma - 1)\ln\frac{T}{T_0}. \tag{6}$$

Transistor T_4 works at a PTAT^2 current , so:

$$\left|V_{GS4}(T)\right| = V_{FB} + E_{G0} + \frac{V_{GS}(T_0) - V_{FB} - E_{G0}}{T_0} T + \frac{nkT}{q}\gamma\ln\frac{T}{T_0}. \tag{7}$$

Considering equations (6) and (7), the superior-order correction voltage will have the following expression:

$$V_{SUP}(T) = -\frac{nkT}{q}\ln\frac{T}{T_0}. \tag{8}$$

By a proper biasing of the MOS transistor from the zero-order curvature-corrected voltage reference, this term will compensate the logarithmic dependent on temperature term from $V_{GS}(T)$ (included in ZVR block), resulting a theoretical zero value of the temperature dependence for the proposed superior-order curvature-corrected voltage reference.

2.5. THE SUPERIOR-ORDER CURVATURE-CORRECTED VOLTAGE REFERENCE

Supposing that the zero-order curvature-corrected is biased at a PTAT current and that the DDS block is biased at PTAT and PTAT^2 currents, respectively (the

generation of this currents will be presented later), the superior-order curvature-corrected voltage reference will have the following expression:

$$\begin{aligned} &V_{REF}(T) = V_{GS}(T) + V_{LIN}(T) + V_{SUP}(T); \\ &V_{REF}(T) = V_{FB} + E_{G0} + \frac{V_{GS}(T_0) - V_{FB} - E_{G0}}{T_0} T + \\ &+ \frac{nkT}{q}(\gamma - 1)\ln\frac{T}{T_0} + \frac{nkT}{q}\ln\left[\frac{(W/L)_2 (W/L)_6}{(W/L)_3 (W/L)_5}\right] - \frac{nkT}{q}\ln\frac{T}{T_0}. \end{aligned} \tag{9}$$

The linear correction is obtained for:

$$\frac{V_{GS}(T_0) - V_{FB} - E_{G0}}{T_0} + \frac{nk}{q}\ln\left[\frac{(W/L)_3 (W/L)_6}{(W/L)_2 (W/L)_5}\right] = 0, \tag{10}$$

while the superior-order curvature-correction is achieved because of the usual value of the technological parameter $\gamma = 2$. By implementing both linear and superior-order curvature-corrections, the reference voltage will have a theoretical zero value of the temperature coefficient:

$$V_{REF}(T) = V_{FB} + E_{G0} \cong 1.2 \text{ V}. \tag{11}$$

The great advantages of the previous presented circuit are:

– The exclusively use of the MOS active devices, allowing an important decreasing of the silicon area;

– The low-voltage operation as a result of replacing the classical MOS transistors by a DTMOS active device;

– The low-power operation obtained by a weak inversion of all MOS transistors from the circuit;

– The very small value of the temperature coefficient (theoretical zero) achieved by implementing two curvature-corrections, linear and logarithmical.

2.6. THE AUXILIARY CURRENT REFERENCE (ACR)

The goal of this block is to generate two currents: I_0, which is, in a first-order approximation, independent on temperature and I_1, with a PTAT variation. Because of the logarithmical dependence $V_{GS}(I_D)$ for a MOS transistor working in weak inversion, the small errors from the linear temperature dependence of the PTAT current or in the temperature dependent current will be strongly reduced. So, any simple circuit using exclusively MOS active devices working in weak inversion could be used for implementing the auxiliary current reference.

2.7. THE CURRENT SQUARER CIRCUIT

In order to obtain I_2 current with PTAT^2 dependence for polarizing the Asymmetric Differential Amplifier, a current multiplier using subthreshold-operated MOS transistors will be presented in Fig. 3.

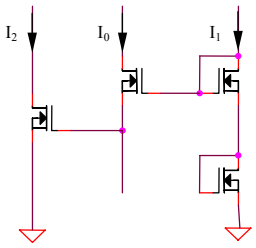

Fig. 3 – The current squarer circuit.

The relation between the circuit currents is $I_2 = I_1^2 / I_0$. So, I_2 will have a PTAT^2 dependence.

2.8. THE SECOND-ORDER ERRORS

The most important cause of errors for the proposed superior-order curvature-corrected voltage reference is represented by the temperature dependence of the I_0 current, supposed to be independent on temperature, in a first-order analysis. Because this current is generated by a first-order curvature-corrected current reference, its real temperature dependence will be given by a logarithmical dependent on temperature term, similar to the last term from (1). The errors introduced by the second-order effects could be quantitative evaluated by the error ε :

$$\varepsilon(T) = \frac{nkT}{q}\left[\frac{nk}{qE_{G0}}(T - T_0) - \frac{nk}{2qT_0E_{G0}}(T - T_0)^2\right]. \tag{12}$$

A proper changing in the aspect ratios of T_2 and T_3 transistors from Fig. 2 can remove the linear term from (12) (that is equivalent with a small variation of the PTAT voltage necessary for the linear correction). The quadratic term from (12) will be concretized in an insignificant temperature coefficient of the superior-order curvature-corrected voltage reference:

$$TCR = \left(\frac{V_{t0}}{E_{G0}T_0}\right)^2 (T - T_0). \tag{13}$$

For example, for an extended temperature range between $263\,K$ and $363\,K$, TCR will have an extremely small value, 0.53 ppm/K.

3. **SIMULATED RESULTS**

The SPICE simulation $V_{REF}(T)$ based on $0.35\,\mu$m CMOS technology parameters and on models associated to Virtuoso package from Cadence are presented in Fig. 4. The supply voltage is $V_{DD} = 2.5$ V. The most important MOS parameters used in the previous simulations are: $V_{Tn} = 0.4$ V, $V_{Tp} = -0.5$ V. The simulated temperature coefficient of the voltage reference is $\mathrm{TCR} = 9.4$ ppm/K for an extended temperature range of $173\,\mathrm{K} < T < 423\,\mathrm{K}$.

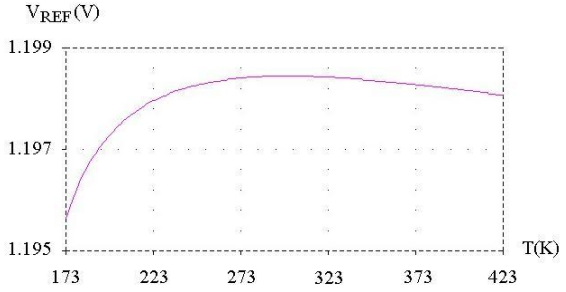

Fig. 4 – SPICE simulation $V_{REF}(T)$ for the square-root curvature-corrected bandgap reference.

4. **CONCLUSIONS**

A new superior-order curvature-corrected voltage reference has been presented. In order to improve the temperature behavior of the circuit, a double differential structure has been used, implementing the linear and the superior-order curvature corrections. An original CTAT (ComplemenTary with Absolute Temperature) voltage generator has been proposed, using exclusively MOS transistors biased in weak inversion for a low power operation of the voltage reference, having two great advantages: an important reducing of the circuit silicon area and an improved accuracy. The superior-order curvature-correction has been implemented by taking the difference between two gate-source voltages of subthreshold-operated MOS transistors, biased at drain currents having different temperature dependencies: PTAT (ProporTional with Absolute Temperature) and

PTAT^2. In order to obtain a low-voltage operation of the circuit, the classical MOS transistor, which implements the zero-order compensated voltage reference, has been replaced by a DTMOS (Dynamic Threshold MOS) transistor. The SPICE simulations confirm the theoretical estimated results, showing a temperature coefficient under 9.4 ppm/K for an extended input range $173\ \mathrm{K} < T < 423\ \mathrm{K}$ and for a supply voltage of $2.5\,V$ and a current consumption of about $1\,\mu A$.

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