EXPERIMENTAL AND THEORETICAL PROOFS FOR THE JUNCTION FIELD EFFECT TRANSISTOR WORK REGIME OF THE PSEUDO-MOS TRANSISTOR

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The dedicated application of the pseudo-MOS transistor is the SOI materials electrical characterization, with the advantage of a nondestructive technique. Also, the pseudo-MOS transistor is an excellent tool for new tests revealed in the SOI devices development. This paper presents an infrequent work regime, encountered in some special biases conditions of the pseudo-MOS transistor. Whether the gate voltage is applied so that the SOI film begins to be depleted, before the inversion onset, a continuous source-drain neutral channel exists at the upper part of the film. The drain current is depending on the drain-source voltage and simultaneously is modulated by the gate action. Consequently, this work regime is a JFET-like behavior. The paper brings some original arguments to highlight this particular work regime.

1. INTRODUCTION

The Pseudo-MOS transistors can be accomplished on all SOI (Silicon On Insulator) wafers, avoiding the photo-lithographic stages [1]. The main application of the pseudo-MOS transistor is the in situ electrical characterization of the SOI materials, being a non-destructive technique [2]. Besides to the classical MOS devices, the pseudo-MOS transistor is a flexible SOI device, suitable for new applications: biodevices [3], optical sensors [4], cMOS circuitry [5], nanodevices, [6].

Frequently, the pseudo-MOS transistor is working as an upside down MOSFET transistor, with an inversion channel thru the SOI film bottom. Usually the source and drain are represented by two metallic probes placed onto the upper film. The gate command is ensured by the substrate terminal contact, as a backgate [7]. This device is a perfect candidate for the SOI interfaces electrical characterization [8].

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This paper highlights a new aspect of the pseudo-MOS work regimes. The device has a MOSFET like behavior in strong inversion or in strong accumulation, but in the depletion regime, a source-drain current is ensured by the majority carriers that still exist in the upper neutral region of the film. This current is modulated by the gate action. An increasing gate voltage, which reinforces the film depletion, leads to a thinner neutral film, as in the case of a JFET (Junction Field Effect Transistor) [9] – exerting its field effect in both cases. The superior neutral channel existence is well-known as a transient situation toward the inversion onset, but its associations with a JFET behavior wasn’t reported yet. This paper studies and proofs this infrequent work regime for the pseudo-MOS transistor – like a JFET – that uses the neutral channel from the film surface.

2. THE DEVICE PRESENTATION AND ITS INFREQUENT WORK REGIME

The pseudo-MOS structure is presented in Fig. 1, with the gate, G, on the bottom of the SOI wafer and the source S and drain D on the top of the film, consisting in two wires. The gate is negative biased, to deplete and eventually to invert the $n$-type SOI film. Hence, a substrate depletion arises, too.

Consequently, the inferior part of the SOI film contains a depleted region, with positive ions, and the superior part of the film is still neutral. In this situation, a current flow from source to drain is possible. The following notations are used: $I_D$ – the drain current, $V_{DS}$ – the drain-source voltage given by $V_{DS} = V_D - V_S$, and $V_{GS}$ – the gate voltage as $V_{GS} = V_G - V_S$. For low $V_{DS}$ voltages, a linear dependence $I_D - V_{DS}$ is expected, as in the case of JFET transistors. If $V_{DS}$ increases, a quasi-
linear $I_D-V_{DS}$ dependence, followed by a saturation of the output characteristics is expected.

The transfer characteristics stand for the $I_D-V_{GS}$ dependence that is valid between two limits, exactly as in the case of a JFET. The first boundary voltage defines a fully neutral film between source and drain, which is the same condition as the energetic flat bands in the SOI film. Therefore, this first limit is well described by the flat band voltage, $V_{FB}$ [10]. The second boundary voltage defines a maximum depleted SOI film or a minimum neutral channel. The partially-depleted SOI structures offer minimum neutral channel beginning with the inversion onset. The fully-depleted SOI structures, as their name assert, can be completely depleted under the gate action, without neutral channel. In both structures, this maximum depletion occurs when the inversion conditions appears, so for a threshold voltage, $V_T$ [10], applied on the gate terminal, as a second limit.

In order to offer the devices similarity proof, the following work hypotheses are taken into account: (1) all the real effects concerning the interfaces properties are focused on one global model parameter – the flat band voltage, $V_{FB}$; (2) in the theoretical approaches the flat band voltage is assumed zero as in an ideal structure; (3) the flat band voltage and the threshold voltage are extracted for the real SOI measured structure and added to the theoretical model, by superposition; (4) an uniform doping concentration in the $n$-type film and $p$-type substrate is assumed accordingly with the SIMOX technology [1]; (5) the insulator is the silicon dioxide; (6) the source is grounded, $V_S=0V$, in all the cases.

3. THEORETICAL ARGUMENTS

A cross-section through an ideal pseudo-MOS structure, between source – as potential reference and gate – as active electrode, is shown in Fig. 2. It doesn’t matter if the SOI film is fully or partially depleted, because in this analysis, the negative gate voltage anyway allows a neutral region, in the left part of the film (Fig. 2).

![Fig. 2 – A segment from the pseudo-MOS transistor structure.](image-url)
The main notations are: $q$ – elementary electrical charge; $N_D$ – doping concentration in $n$-type film; $N_A$ – doping in $p$-type substrate, $x_{S1,S2}$ – film, respectively substrate thickness; $x_{d1,d2}$ – space charge region thickness in film, respectively in substrate; $x_{BIS}$ – Buried Insulator (BIS) thickness; $\varepsilon_{Si}$ – dielectric permittivity of Silicon, $\varepsilon_{ox}$ – dielectric permittivity of the oxide as buried insulator.

From the potential function continuity at $x_4$ abscissa, results:

$$V_{GS} = \phi_{SOI} + \phi_{BIS} + \phi_{SB}, \quad (1)$$

where $\phi_{SOI}$ is the potential drop over the $n$-type SOI film that actually falls on the depleted region, $\phi_{BIS}$ is the potential drop over the buried insulator and $\phi_{SB}$ is the potential drop over substrate. By Poisson’s equation integration, in one-dimensional form, considering the depletion approximation for the silicon film and substrate, the prior potential drops result:

$$\phi_{SOI} = -\frac{qN_D}{\varepsilon_{Si}} \frac{x_{d1}^2}{2}, \quad (2)$$

$$\phi_{BIS} = -\frac{qN_p}{\varepsilon_{ox}} x_{d1} x_{BIS}, \quad (3)$$

$$\phi_{SB} = -\frac{qN_A}{2\varepsilon_{Si}} x_{d2}^2. \quad (4)$$

The computing methodology is similarly as for thin SOI films [11, 12]. Replacing (2), (3), (4) in (1), and taking into account the conservation of the electric charge in structure, an algebraic II$^{nd}$ degree equation with $x_{d1}$ unknown, results. Solving this equation, the extensions of the space charge regions $x_{d1}$ versus $V_{GS}$ and material parameters is computed:

$$x_{d1} = \frac{\varepsilon_{Si}}{\varepsilon_{ox}} x_{BIS} + \sqrt{\left(\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\right)^2 x_{BIS}^2 - \left(\frac{1}{N_D} + \frac{1}{N_A}\right)^2 qN_D V_{GS}} \cdot \varepsilon_{Si} \frac{2}{N_D N_A} \quad (5)$$

With the previous expression (5), the thickness of the neutral channel can be computed versus the modulator gate voltage, as $x_{S1}$–$x_{d1}$. Hence, the static characteristics can be estimated for an applied drain-source voltage. In the linear work regime, at low $V_{DS}$, the neutral channel has a roughly uniform width from source to drain (Fig. 3).
So, the static characteristics are given by the Ohm's law:

\[ I_D = \beta_{PS} V_{DS} \cdot \left( 1 - \frac{x_{d1}}{x_{S1}} \right), \quad (6) \]

where \( \beta_{PS} \) is a geometrical factor of the pseudo-MOS transistor, [13], modeled in this case with:

\[ \beta_{PS} = qN_D \cdot \frac{Z}{L} \cdot \mu_n x_{S1}, \quad (7) \]

where \( Z \) is the depth of the neutral film, \( L \) is the length of the neutral film and \( \mu_n \) is the electrons mobility in the \( n \)-type neutral film (Fig. 3).

A cross-section through a Junction Field Effect Transistor JFET and the applied voltages that ensure the current flow in the \( n \)-neutral channel, are presented in Fig. 4.
In the same regime, the static characteristics of a Junction Field Effect Transistor JFET are [10]:

$$I_D = \beta_{\text{JFET}} V_{DS} \left(1 - \frac{2 \epsilon_{Si} \phi_{B0}}{q N_D x_{S1}^2} (\phi_{B0} - V_{GS}) \right),$$  \hspace{1cm} (8)

where the JFET notations $x_{S1}, x_{d1}, N_A, N_D, \epsilon_{Si}, V_{GS}$ preserve the same significance as for the pseudo-MOS transistor (Fig. 3 and Fig. 4). Additionally, for the JFET transistor, $\phi_{B0}$ is the internal build-in potential and the geometrical factor has a quite similar expression as for pseudo-MOS:

$$\beta_{\text{JFET}} = q N_D \frac{Z}{L} \mu_a \cdot (2 x_{S1}) \cdot$$  \hspace{1cm} (9)

This linear model is valid for low $V_{DS}$. For higher drain voltage, the neutral channel will narrow from source to drain. After an integration operation along the neutral channel from $y = 0$ to $y = L$ that is equivalent from $V_S$ to $V_D$, the drain current results. The $I_D$ current tends to depend on $V_{GS}$ via $\phi_{\text{SOI}}$ that depends on $x_{d1}^2$ from (2), and $x_{d1}$ depends on $V_G^{1/2}$ from (5). Hence the static characteristics in quasi-linear region, presents a drain current dependence on the voltages $V_{DS}^{3/2}$ and $V_{GS}^{3/2}$ for the pseudo-MOS transistor, as for the JFET transistor [9].

This behavior in quasi-linear regime, beside to the similar analytical models (6) and (8) stands for an theoretical argument to sustain the JFET like behavior, of the pseudo-MOS transistor, biased in the depletion regime. Also, the analytical model (6) represents a starting point for the PSpice description of the device for different applications [14].

4. EXPERIMENTAL CONSIDERATIONS

In this paragraph the experimental measurements were performed with a pseudo-MOS transistor made on a SOI wafer manufactured by SIMOX technique with: $N_D = 5 \times 10^{15} \text{ cm}^{-3}, N_A = 10^{15} \text{ cm}^{-3}, x_{S1} = 0.2 \mu\text{m}, x_{BIS} = 0.4 \mu\text{m}$.

For the experimental tests, only fully-depleted SOI structures were available. The experimental device set-up is presented in Fig. 5. The source and drain contacts were two probes placed onto SOI film and the substrate contact acts as gate. The channel length is given by the source-drain distance that was $L = 5\text{mm}$. 
For $V_{DS} = 0.1V, 0.2V, 0.3V$ the current recording was measured with a picoampermeter, Keithley 236. Figure 6 presents the experimental transfer characteristics when $-10V < V_{GS} < +15V$.

During the gate voltage augmentation the pseudo-MOS transistor passes from the strong inversion regime at high negative voltages, toward the JFET like regime during the depletion regime and finally to the MOSFET like behavior during the accumulation regime. The most relevant behavior as JFET happens for $V_{FB} < V_{G} < V_{T}$.

Figure 6a shows the measured currents corresponding to the negative $V_{GS}$ voltage on a separate axis in order to make possible the threshold voltage extraction from the incipient depletion up to strong inversion regime. For a similar scope, the positive $V_{GS}$ curves are separately represented in order to offer the flat-band voltage. For this SOI structure, the following model parameters are extracted: $V_{T} = -4V, V_{FB} = +1V$, establishing the boundary between depletion and inversion regime for $V_{T}$ and depletion and accumulation regime for $V_{FB}$ [2, 8]. Hence, the gate voltages range that ensures a neutral channel existence in the upper part of the SOI film, is $-4V < V_{GS} < +1V$. In Fig. 6a isn’t visible a variation of the current versus the gate voltage due to tiny values. Therefore, a secondary axis selection for the current values at logarithmic scale, inside the range $-4V < V_{GS} < +1V$, is available in Fig. 6b.

The currents values are small due to the particular geometrical factor with a long distance between the source and drain contacts that provides a high resistive trace, besides to the parasitic Schottky contacts. Consequently, the transfer characteristics for the pseudo-MOS transistor in the depletion regime, where the JFET-like effect is highlighted, are separately presented in Fig. 7.
Fig. 6 – The experimental $I_D-V_{GS}$ curves for different $V_{DS}$ voltages: a) the global characteristics with principal axis (right) for positive $V_{GS}$ voltages and secondary axis for negative $V_{GS}$ voltages (left); b) detail on secondary axis when the neutral channel exists (left axis) and all the others regimes on the right axis.

Fig. 7 – The transfer characteristics, $I_D-V_{GS}$, of the pseudo-MOS transistor, at given $V_{DS}$. Here is obvious the parabolic shape of these characteristics, as in the case of the junction field effect transistor [9].

A comparison between some experimental measurements – points – and the presented analytical model (6) – lines – is exposed in figure 8, for the output characteristics. Two values of the gate voltage: $-3.1V$, $-4.1V$, were considered. From Fig. 8 can be observed a better agreement between analytical curves and
measured curves for $V_{GS} = -3.1$V. This is previsible because the analytical model is focused just on the JFET current component. For increased gate voltages, respectively for $V_G = -4.1$V, the JFET current decreases and a subthreshold current begin to flow through the inversion channel from the SOI-BIS interface. The picoamperometer measures the superposition of both currents, as the total drain current.

![Fig. 8 – A comparison between analytical model and some experimental points for the output characteristics.](image)

5. CONCLUSIONS

This paper presented a new aspect of the pseudo-MOS working regime. During the SOI film depletion, the device has a junction field effect JFET-like behavior. This is accomplished by the gate modulation of the neutral channel placed between source and drain. An analytical model for a pseudo-MOS transistor working in JFET regime was presented. This model proves that the pseudo-MOS has quite similar expressions for the drain current versus $V_{DS}$ and $V_{GS}$ voltages as a JFET. An increased gate voltage provides an intensification of the inversion current that finally overcomes the volume current and prevails at high negative voltages.

The experimental device, being a fully-depleted SOI structure with a long channel, offers very low currents, almost invisible at a global scale. By a proper selection of the current axis during the neutral channel existence, a quite parabolic $I_D-V_{GS}$ curve was recorded for the pseudo-MOS transistor. The limitation of the
experimental set-up comes from the impossibility of the electrons and holes currents separation, measuring all the time the total current by their superposition. For higher drain voltages, a narrow neutral channel appears from source to drain, in the same manner as for JFET.

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