SIMPLE BICMOS REALIZATION OF FULL BALANCED VOLTAGE DIFFERENCING BUFFERED AMPLIFIER

WORAPONG TANGSRIRAT

Key words: Full balanced-voltage differencing buffered amplifier (FB-VDBA), BiCMOS technology, Integrated circuit.

This paper presents an alternative circuit configuration for realizing the recently introduced active building block, namely full balanced voltage differencing buffered amplifier (FB-VDBA), eminently suitable for integration in BiCMOS technology. The proposed FB-VDBA consists of a fully differential transconductor as an input stage, and the voltage buffer and inverter as output stages. The circuit has been designed using bipolar and MOS transistors, in order to achieve the advantages of the both technologies. Using single FB-VDBA, one resistor and one capacitor, the voltage-mode all-pass filter is constructed for the specific application of the designed active element. PSPICE simulation results, obtained by using the real transistor parameters of the standard 0.35 μm BiCMOS technology, are performed to confirm the performances of the proposed circuit and its application.

1. **INTRODUCTION**

In the last decade, new circuit ideas of active building blocks for providing the potentiality in analog signal processing circuit design have received much attention [1]. A number of publications concerning with this area has continuously interesting, in order to provide further circuit characteristic improvements, and obtain more effective and interesting circuits [2–11]. In [1], the present-day active elements and several new active building blocks are reviewed and introduced. One of them is the newly introduced active element named full balanced voltage differencing buffered amplifier (FB-VDBA) [2]. Many interesting applications of FB-VDBA in mainly analog signal processing and signal generation circuits were also introduced in [2–5], to demonstrate the usefulness and easy implementation in fully-balanced structures. The given survey [2] shows that the FB-VDBA implementation can be achieved by using two integrated circuits OPA860 [12].

The purpose of this communication is, therefore, to introduce the FB-VDBA implementation suitable for integration in 0.35 μm BiCMOS technology and

King Mongkut's Institute of Technology Ladkrabang (KMITL), Faculty of Engineering, Bangkok 10520, Thailand, E-mail: drworapong@yahoo.com

Rev. Roum. Sci. Techn. – Électrotechn. et Énerg., **60**, *4*, p. 409–415, Bucarest, 2015

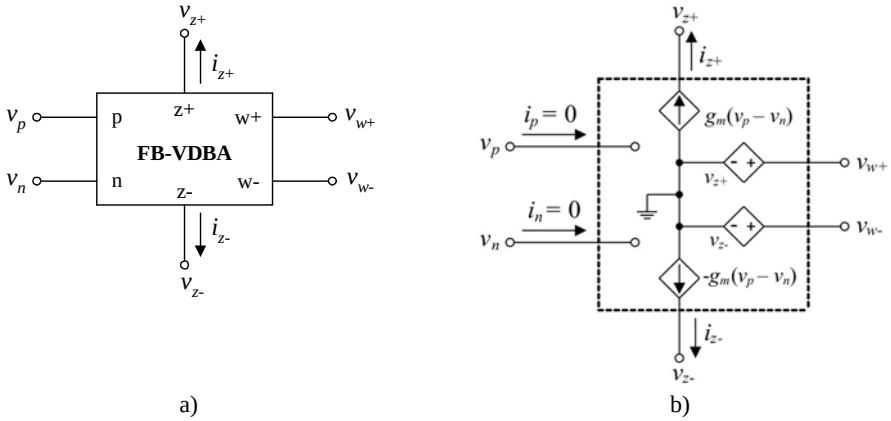
capable of operate at low supply voltages of ± 0.75 V. The proposed FB-VDBA circuit element has a wide bandwidth of 20 MHz with total power consumption of 1.6 mW. The performance of the proposed circuit has been tested with an application example of the first-order voltage-mode all-pass filter. PSPICE simulation results with the real 0.35 μm BiCMOS process parameters are given to verify the workability of the designed circuit element and its application.

2. **PRINCIPLE OF FB-VDBA**

The schematic symbol of the FB-VDBA and its equivalent circuit are depicted in Fig.1a and 1b, respectively. Its terminal characteristics can be described by the following set of circuit expressions [2]:

$$\begin{bmatrix} i_{z+} \\ i_{z-} \\ v_{w+} \\ v_{w-} \end{bmatrix} = \begin{bmatrix} g_m & -g_m & 0 & 0 \\ -g_m & g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_{z+} \\ v_{z-} \end{bmatrix}, \tag{1}$$

where g_m is the transconductance gain of the FB-VDBA.



a) b)

Fig. 1 – FB-VDBA [2]: a) schematic symbol; b) its equivalent circuit.

According to (1) and Fig. 1(b), the FB-VDBA device has a pair of high-impedance differential voltage inputs (p and n), and a pair of high-impedance current outputs (z+ and z–), as well as two low-impedance voltage outputs (w+ and w–). This means that the FB-VDBA element is conceptually a combination of the transconductance amplifier as an input stage, and the unity-gain voltage buffer as an output stage. The differential input voltage between the terminals p and n ($v_p - v_n$) is then converted to currents at terminals z+ and z– (i_{z+} and i_{z-}) by a g_m parameter,

with equal value but opposite directions. The output voltages v_{w+} and v_{w-} will follow the voltages across terminals z+ and z–, respectively. In this way, the utilization of voltage inverter is not required for the voltage inversion purpose.

3. **PROPOSED BICMOS FB-VDBA REALIZATION**

The complete schematic diagram of the proposed BiCMOS FB-VDBA circuit is shown in Fig. 2. The input stage consists of input transistors (M_1–M_2 and Q_1–Q_4) and current mirror transistors (Q_5–Q_7, Q_8–Q_{10}, Q_{11}–Q_{12} and Q_{13}–Q_{14}), where I_A and I_B are the external dc biasing currents. Transistors M_3–M_6 and M_7–M_{10} represent the output stages, which provide w+ and w– terminals respectively.

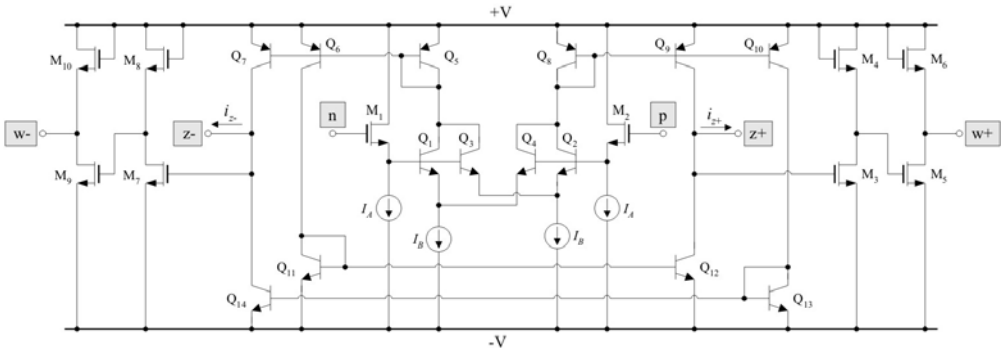


Fig. 2 – Complete diagram of the proposed BiCMOS FB-VDBA.

Group of input transistors (M_1–M_2 and Q_1–Q_4) act as the transconductance amplifier that converts the differential input voltage (v_p–v_n) into the signal currents flowing through the collectors of Q_5 and Q_8. The MOS input transistors M_1 and M_2 provide very high input impedance and very low bias currents. Because of their low transconductance, the bipolar input transistors Q_1–Q_4 are added to provide an extra gain stage. The mirror stages (Q_5–Q_7, Q_8–Q_{10}, Q_{11}–Q_{12} and Q_{13}–Q_{14}), will convey the signal currents i_{c5} and i_{c8} to ports z+ and z–, respectively. The small-signal effective transconductance (g_m) of the FB-VDBA derived from this stage can be calculated in a fashion similar to that for the all bipolar version [13], giving:

$$g_m = \frac{I_B}{V_T}, \tag{2}$$

where $V_T \cong 26$ mV at 27 °C is the thermal voltage. From (2), it is noted that the value of g_m is tunable electronically and linearly through the basing current I_B.

For the output stages, transistors M_3–M_6 and M_7–M_{10} form the cascaded common-source amplifier with diode connected load [8]. The small-signal effective

voltage gain (v_{w+}/v_{z+} and v_{w-}/v_{z-}) can be determined by using hybrid π model in which both the body effect and the output resistance of the two transistors have been included. Assume that all transistors operate in the active region. Therefore, the resulting voltage gains in Fig. 2 are approximately found as:

$$\frac{v_{w+}}{v_{z+}} \cong \frac{g_{m3}}{g_{m4}} \frac{g_{m6}}{g_{m5}} \tag{3}$$

$$\frac{v_{w-}}{v_{z-}} \cong \frac{g_{m7}}{g_{m8}} \frac{g_{m9}}{g_{m10}} \quad , \tag{4}$$

where g_{mi} denotes the conductance of transistor M_i (i = 1, 2, ..., 10). Under the simplifying assumption that all the transistors have the same conductance values ($g_m \cong g_{mi}$), thus $v_{w+} \cong v_{z+}$ and $v_{w-} \cong v_{z-}$ as expected.

4. **SIMULATION RESULTS**

For the purpose of the performance verification of the proposed FB-VDBA realization in Fig. 2, the circuit was simulated on PSPICE program using standard 0.35 μm BiCMOS process parameters. The aspect ratios (W/L in μm/μm) of the transistors were selected as: 14/0.7 and 56/0.7 for M_1–M_2 and M_3–M_{10}, respectively. The sufficiently high W/L ratio of transistors M_3–M_{10} ensures a low-output resistance of the buffer stages, thereby avoiding the loading effect. The circuit was biased at I_A = 25 μA under $\pm V$ = ± 0.75 V.

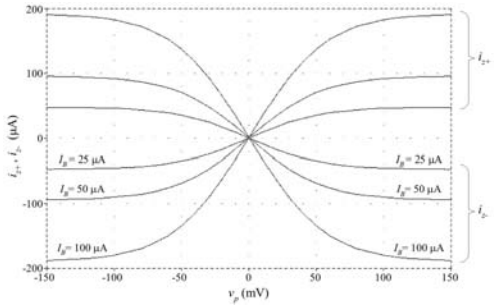


Fig. 3 – Dc transfer characteristics of i_{z+}/v_p and i_{z-}/v_p.

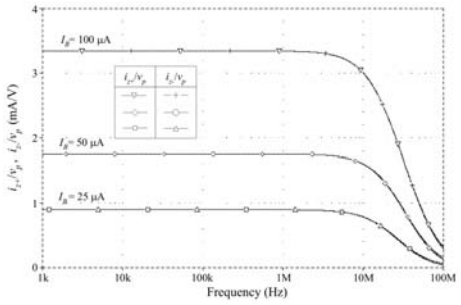


Fig. 4 – Ac transfer characteristics of i_{z+}/v_p and i_{z-}/v_p.

The dc simulation results of the transconductance gain of the proposed FB-VDBA for three different values of I_B (i.e., I_B = 25 μA, 50 μA and 100 μA) have been plotted in Fig. 3. The simulated frequency responses of the transconductance gain from port p to ports z± have been plotted in Fig.4. From the results, the –3dB bandwidth (f_{-3dB}) are located at 20 MHz, 22 MHz and 23 MHz, respectively.

Figure 5 shows the dc voltage transfer characteristics, which is almost –0.4 V to + 0.4 V within 0.3 % error at the end of the transfer curves. The ac voltage gains for the voltage transfer characteristics $v_{w\pm}/v_{z\pm}$ are plotted in Fig. 6. The voltage gain of 0.986 and the f_{-3dB} of 1.3 GHz have been obtained. Thus, the maximum operating frequency for the proposed FB-VDBA in Fig. 2 is $f_{max} \cong \min(f_{-3dB}) \cong 20$ MHz. In addition, the proposed circuit has 1.6 mW static power consumption.

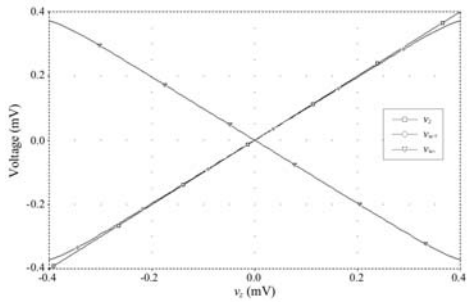


Fig. 5 – Dc transfer characteristics of v_{w+}/v_z and v_z/v_{w-}.

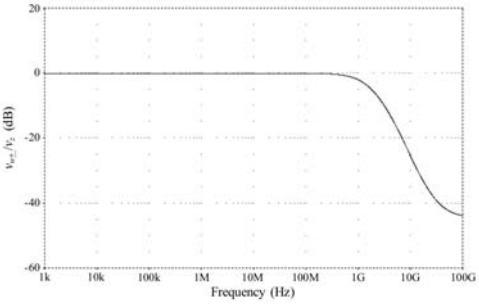


Fig. 6 – Ac transfer characteristics of v_{w+}/v_z and v_{w-}/v_{z-}.

5. **EXAMPLE OF FB-VDBA APPLICATION**

An application example of the proposed FB-VDBA is shown on the design of first-order voltage-mode all-pass filter, using a single FB-VDB along with two passive components (one resistor and one capacitor) as shown in Fig. 7 [3]. Circuit analysis of Fig. 7 results in the following voltage transfer function:

$$\frac{V_o(s)}{V_{in}(s)} = \frac{1 - sRC}{1 + \dfrac{sC}{g_m}} \quad . \tag{5}$$

From (5), if the condition $R = 1/g_m$ is fulfilled, the circuit of Fig. 7 performs the first-order voltage-mode all-pass filter with the following pole frequency (f_p) and phase response (ϕ):

$$f_p = \frac{1}{2\pi RC} \quad , \tag{6}$$

and

$$\phi = \pi - 2\tan^{-1}(2\pi fRC) \quad . \tag{7}$$

To verify the functionality of the FB-VDBA based all-pass filter realization in Fig. 7, the simulations are also performed with the following active and passive components: I_B = 25 μA, R = 1 kΩ and C = 1 nF, to obtain a first-order all-pass

voltage response with the pole frequency of $f_p \cong 159$ kHz. Fig. 8 shows the simulated gain and phase responses of the filter, when compared with the ideal responses obtained from an equivalent circuit of Fig. 1b. Note that the simulated results are in conformity with the theory. The simulated transient responses are also shown in Fig. 9. This causes the time shift of 1.7 μs at the filter output corresponding to the phase shift of about 96.50°.

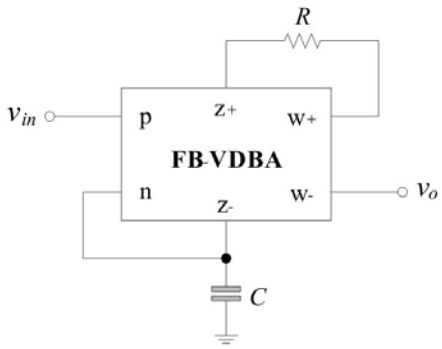


Fig. 7 – First-order all-pass filter using FB-VDBA.

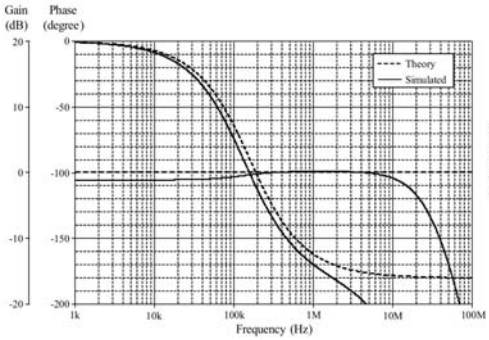


Fig. 8 – Theoretical and simulated gain and phase responses of Fig. at f_p = 159 kHz.

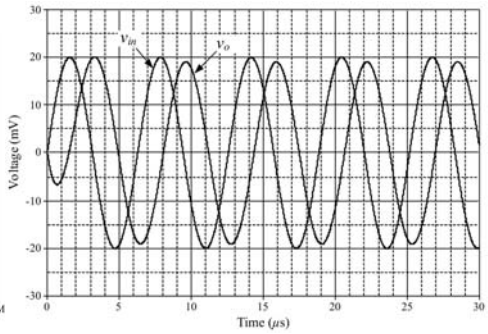


Fig. 9 – Simulated transient responses for the all-pass filter in Fig. 7 at f_p = 159 kHz.

6. **CONCLUSION**

The circuit technique for implementing a recently introduced active building block, named full balanced voltage differencing buffered amplifier (FB-VDBA), is introduced in this study. Our main objective is to describe the simple realization of FD-VDBA, which is suitable for fabricating in BiCMOS technology. As an application example, the usability of the realized active circuit element has been shown on the first-order voltage-mode all-pass filter realization. The performance

of the proposed FD-VDBA is discussed and also verified by PSPICE simulations using real 0.35 μm BiCMOS process parameters.

ACKNOWLEDGEMENTS

The research described in this work is supported by Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL).

Received on March 30, 2015

REFERENCES

1. D. Biolek, R. Senani, V. Biolkova, Z. Kolka, *Active elements for analog signal processing: classification, review, and new proposals*, Radioengineering, **17**, *4*, pp. 15–32, 2008.
2. V. Biolkova, Z. Kolka, D. Biolek, *Fully balanced voltage differencing buffered amplifier and its applications*, Proc. 52nd MWSCAS, Aug. 2–5, Cancun, Mexico, pp. 45–48, 2009.
3. D. Biolek, V. Biolkova, Z. Kolka, *All-pass filter employing fully balanced voltage differencing buffered amplifie*, Proc. IEEE Latin American Sym. Circuits and Systems (LASCAS-2010), Iguacu, Brasil, pp. 232–235, 2010.
4. J. Bajer, D. Biolek, V. Biolkova, Z. Kolka, *Voltage-mode balanced-outputs quadrature oscillator using FB-VDBAs*, Proc. 22nd Int. Conf. Microelectron. (ICM 2010), Cairo, Egypt, pp. 491–494, 2010.
5. R. Sotner, J. Jerabek, N. Herencsar, *Voltage differencing buffered/inverted amplifiers and their applications for signal generation*, Radioengineering, **22**, *2*, pp. 490–504, 2013.
6. J. Jin, C. Wang, *Current-mode four-phase quadrature oscillator using current differencing transconductance amplifier based first-order allpass filter*, Rev. Roum. Sci. Techn.– Électrotechn. et Énerg., **57**, *3*, pp. 291–300, 2012.
7. J. Jin, P. Liang, *Resistorless current-mode quadrature oscillator with grounded capacitors*, Rev. Roum. Sci. Techn.– Électrotechn. et Énerg., **58**, *3*, pp. 304–313, 2013.
8. N. Herencsar, S. Minaei, J. Koton, E. Yuce, K. Vrba, *New resistorless and electronically tunable realization of dual-output VM all-pass filter using VDIBA*, Analog Integr. Circ. Signal Process., **74**, *1*, pp. 141–154, 2013.
9. W. Tangsrirat, S. Unhavanich, *Signal flow graph realization of single-input five-output current-mode universal biquad using current follower transconductance amplifiers*, Rev. Roum. Sci. Techn.– Électrotechn. et Énerg., **59**, *2*, pp. 183–191, 2014.
10. J. Jerabek, R. Sotner, K. Vrba, *Electronically adjustable triple-input single-output filter with voltage differencing transconductance amplifier*, Rev. Roum. Sci. Techn.– Électrotechn. et Énerg., **59**, *2*, pp. 163–172, 2014.
11. W. Tangsrirat, O. Channumsin, T. Pukkalanun, *Single current-controlled sinusoidal oscillator with current and voltage outputs using single current-controlled current conveyor transconductance amplifier and grounded passive elements*, Rev. Roum. Sci. Techn.– Électrotechn. et Énerg., **60**, *2*, pp. 175–184, 2015.
12. *** *OPA860-Wide bandwidth operational transconductance amplifier* (*OTA and buffer*), Texas Instruments, SBOS331C, June 2005.
13. W. Tangsrirat, *Single-input three-output electronically tunable universal current-mode filter using current follower transconductance amplifiers*, Int. J. Electron. Commun. (AEU), **65**, *10*, pp.783–787, 2011.