2.4 GHZ LOW POWER UP-CONVERSION MIXER USING NOVEL CURRENT-MIRRORS

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Key words: CMOS, Radio frequency, Wireless sensor network (WSN), Mixer, Current-reuse current-mirror, Low voltage, Low power.

A 2.4 GHz CMOS up-conversion mixer using novel current mirrors based on chartered 0.18 μm RF CMOS technology for 2.4 GHz wireless sensor network (WSN) application is presented in this paper. The current-reuse current-mirror and current-bleeding technique are used in the driver and switching stages of the mixer, respectively. The post-layout simulation results demonstrate that the novel up-conversion mixer can provide about 10.5 dB conversion gain with a local oscillator (LO) power of 0 dBm, while the power consumption is only 0.25 mW with 1 V supply voltage, and the 1 dB compression point and input-referred third-order intercept point (IIP3) of the mixer are 10.32 dBm and 2.66 dBm, respectively. The chip area including test pads is only 0.5 × 0.6 mm^2. Comparing with the previously reported mixers, the proposed mixer has the advantages of lower supply voltage, lower power consumption, higher linearity and smaller chip area than most of the other reported works.

1. **INTRODUCTION**

Wireless sensor network (WSN) is a self-organizing network system deployed in monitoring areas by large amounts of cheap miniature sensor nodes. These nodes are designed for data collecting, processing and transmitting in applications such as home automation, industrial control, public security, environmental monitoring and so on [1]. WSN is an application of extreme low power consumption, low voltage low power WSN nodes with less power consumption and higher performance integrated circuits (IC) are the urgent need for the further market. Fig.1 is a classic block diagram of an WSN wireless transmitter, the LPF is the low pass filter, the VCO is the voltage controlled oscillator, the BPF is the band pass filter, the PA is the power amplifier, and the I and Q signals stand for a pair of quadrature signals. Just like the oscillators in reference [2], the up-conversion mixer is one of the most important analog blocks in the WSN wireless transmitter, which transforms the

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intermediate frequency (IF) signal into radio frequency (RF) signal, and its performance has significant influence on the whole transmitter.

The reported mixers can be divided into two categories: the passive mixers and the active mixers. Passive mixers have the advantages of better linearity and frequency response, but they have conversion loss and require large local oscillator (LO) signals, which are not the desired features for wireless communication systems. The most popular active mixers are the Gilbert-type [3-10], and they can provide relative large conversion gain and low even-order distortion. However, the reported Gilbert mixers suffer from relatively high voltage and large power dissipation, because the number of stacked transistors and loads are at least three, and it is not suitable for low voltage application.

In this paper, a new CMOS 2.4 GHz up-conversion mixer for 2.4 GHz Wireless sensor network application is presented. The current-reuse current-mirror and current-bleeding techniques significantly decrease the power consumption, and improve the linearity of the mixer. The proposed up-conversion mixer has the advantages of lower supply voltage, lower power consumption, higher linearity and smaller chip area than most of the other reported works.

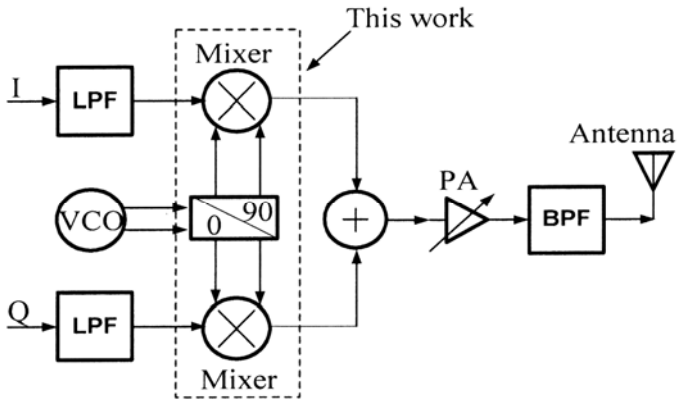


Fig. 1 – Block diagram of an WSN transmitter.

2. **CIRCUIT DESCRIPTION**

2.1 CURRENT-REUSE CURRENT-MIRROR CONFIGURATION

The transconductance driver stage of the up-conversion mixer is a resistor feedback current reuse current-mirror, and the derivations of the current reuse current-mirror are shown in Figs. 2 and 3.

Figure 2a is a traditional NMOS current-mirror. Figure 2b is the improved current-mirror with resistor feedback for the proposed mixer.

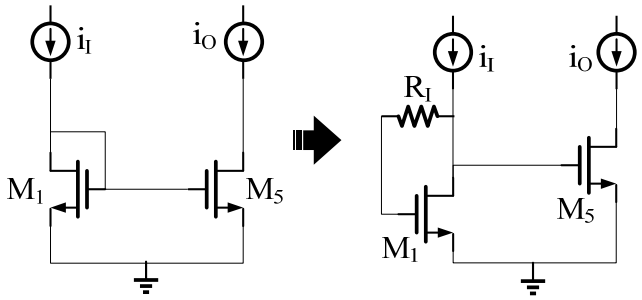


Fig. 2 – The improved current-mirror: a) Traditional NMOS current-mirror; b) The proposed current-mirror.

The current mirror uses the principle that if the gate-source potentials of two identical MOS transistors are equal, the channel currents should be equal [11].

Considering the CMOS model suggested by Sah [12] and used in SPICE by Shichman and Hodges [13], the channel current of MOS transistor can be expressed as:

$$i_D = \frac{\mu_o C_{ox} W}{L}\left[\left(V_{GS} - V_T\right) - \left(\frac{V_{DS}}{2}\right)\right] V_{DS}, \tag{1}$$

where μ_o is the surface mobility of the channel for the n-channel or p-channel device ($cm^2/V{\cdot}s$), and C_{ox} is the capacitance per unit area of the gate oxide (F/cm^2), W and L are the effective channel width and length of the transistor, V_{GS} is the voltage between the Gate and the Source of the MOS transistor, V_{DS} is the voltage between the Drain and the Source of the MOS transistor, and V_T is the threshold voltage of the MOS transistor, respectively.

When the transistor is working in the saturation region (V_{DS} is greater than $V_{DS(sat)}$ or $V_{GS}–V_T$), at this point the current i_D becomes independent of V_{DS}. Therefore, V_{DS} in equation (1) is replaced by $V_{DS(sat)}$ or $V_{GS}–V_T$ to get [11]:

$$i_D = \frac{\mu_o C_{ox} W}{L}\left[\left(V_{GS} - V_T\right)\right]^2, 0 < \left(V_{GS} - V_T\right) < V_{DS}. \tag{2}$$

In Fig.2(a), the gate-source voltage of M_1 is equal to the gate-source voltage of M_5 ($V_{GS(M1)} = V_{GS(M5)}$), and the gate voltage of M_1 is equal to its drain voltage ($V_{G(M1)} = V_{D(M1)}$), and it always satisfies the saturation condition [$0 < (V_{GS(M1)} - V_T) \leq \leq V_{DS(M1)}$], then the input and output currents can be expressed as:

$$i_I = \frac{1}{2}\frac{\mu_o C_{ox} W_1}{L_1}\left[\left(V_{GS} - V_T\right)\right]^2, \tag{3}$$

$$i_O = \frac{1}{2}\frac{\mu_o C_{ox} W_5}{L_5}\left[\left(V_{GS5} - V_T\right)\right]^2. \tag{4}$$

Because $V_{GS(M1)} = V_{GS(M5)}$, if M_1 and M_5 are exactly matched ($W_1/L_1 = W_5/L_5$), we can know that the input current should be equal to the output current

$$i_I = i_O . \tag{5}$$

If M_1 and M_5 are not exactly match ($W_1/L_1 \neq W_5/L_5$), and it is clear that

$$\frac{i_I}{i_O} = \left(\frac{L_1 W_5}{L_5 W_1} \right). \tag{6}$$

From equation (6), we can know that the current gain of the current-mirror can be relatively controlled by the width-to-length ratio of the transistors (M_1 and M_5).

In Fig. 2b, resistor R_1 is connected between the drain and gate of M_1, however, there is no current at the gate of M_1, and there is no current at resistor R_1, the voltages of the both sides of R_1 should be equal. So, in Fig. 2b, we can know that $V_{G(M1)} = V_{D(M1)} = V_{G(M5)}$, and it satisfies $V_{GS(M1)} = V_{GS(M5)}$, and Fig. 2b is also a current-mirror, and its current gain can also be controlled by the width to length ratio of M_1 and M_5.

Figure 3 shows the proposed current-reuse current-mirror technique. The current source i_I in Fig. 2b is replaced by the transistor M_2, and the current source i_O is replaced by the inductor L_1 and capacitor C_3. However, the values of the inductor L_1 and capacitor C_3 should be properly chosen, and the principle is to keep the transistor M_5 working in the saturation region and make the current-reuse current-mirror work properly.

Actually, M_1, M_2 and R_1 consist of a classic resistor feedback current reuse configuration. In the current reuse configuration, stacking a PMOS and a NMOS transistor can increase the equivalent transconductance. Compared with the classic common-source amplifier, the current reuse configuration increases the total transconductance from g_{m1} to ($g_{m1} + g_{m2}$) for the same biasing current [14, 15].

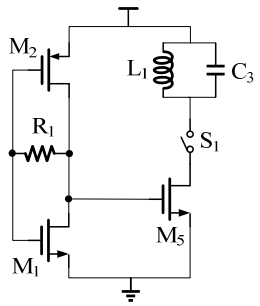


Fig. 3 – The proposed current-reuse current-mirror.

The current reuse stage (M_1, M_2 and R_1) is not only the input stage which provides large transconductance ($g_{m1}+g_{m2}$), but also consists of the new current-

reuse current-mirror with the transistor M_5, and this structure can work in lower supply voltage and provide higher transconductance gain.

2.2. THE PROPOSED UP-CONVERSION MIXER

The proposed mixer is shown in Fig. 4. The mixer consists of two current-reuse current-mirrors. The current-reuse stages (M_1–M_4, R_1 and R_2) are the transconductance input stages, which amplify the received IF voltage signal and transfer them into currents. M_5 and M_6 are connected to the current-reuse stages (M_1–M_4, R_1 and R_2), and they consist of the novel current reuse current-mirrors. The transistors M_7–M_{10} are the NMOS Gilbert switch core, and its function is to modulate the currents provided by the transconductance driver stages. The transistors M_{11} and M_{12} provide the current-bleeding technical for the mixer, which can improve the conversion gain and the input third-order intercept point (IIP3) of the mixer. The two paralleled LC tanks (L_1, C_3 and L_2, C_4) are the output loads of the up-conversion mixer, which act as band-pass filters, and resonate at 2.41GHz, reject the unexpected interference signals.

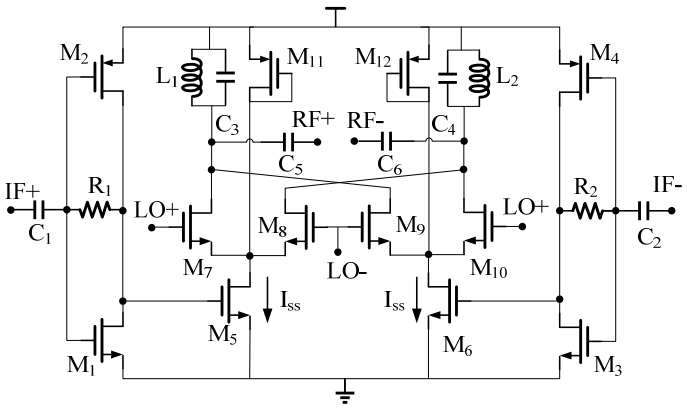


Fig. 4 – The proposed up-conversion mixer.

According to the theory of Gilbert Cell mixer, the conversion gain and IIP3 of the proposed mixer can be approximately expressed as:

$$A_V = \frac{2}{\pi}\left(g_{m7} + g_{m8}\right)\frac{sL_1}{1+s^2L_1C_3} \approx \frac{4}{\pi}\sqrt{\frac{1}{2}\mu C_{ox}\frac{W}{L}I_{SS}}\,\frac{sL_1}{1+s^2L_1C_3}, \tag{7}$$

$$\text{IIP3} = \sqrt{\frac{32I_{SS}}{3\beta_n}}\,. \tag{8}$$

where μ is the surface mobility of the channel for the *n*-channel or *p*-channel device [cm^2/V-s], and C_{ox} is the capacitance per unit area of the gate oxide [F/cm^2], W and L are the effective channel width and length of the transistor.

From equation (7), it is clear that current-reuse current-mirrors make the conversion gain of the mixer increase double. From equations (7–8), we can also know that the conversion gain and the IIP3 of the mixer are proportional to the square root of the bias currents (I_{ss}) flowing in the transistors M_5 and M_6. Because of the current-bleeding technical introduced by M_{11} and M_{12}, the bias currents (I_{ss}) will increase, and the conversion gain and the IIP3 of the mixer will be improved.

3. POST-LAYOUT SIMULATION RESULTS

The proposed up-conversion mixer is realized using Cadence IC Design Tools 5.1.41 Spectre simulator with standard chartered 0.18 μm RF CMOS technology. In the post-layout simulation, the input IF signal is −25 dBm, and its frequency is 10 MHz; the LO signal is 0 dBm, and its frequency is 2.4 GHz.

Figure 5 is the post-layout simulated conversion gain of the mixer versus LO power. From Fig. 5, it is clear that the proposed mixer can provide 10.5 dB conversion gain while the LO power is 8 dBm. However, the conversion gain and the LO power are not the larger the better, too large LO power will deteriorate the linearity of the mixer, for achieving a tradeoff between the LO power, conversion gain and linearity, the 0 dBm LO power is chosen in the post-layout simulation.

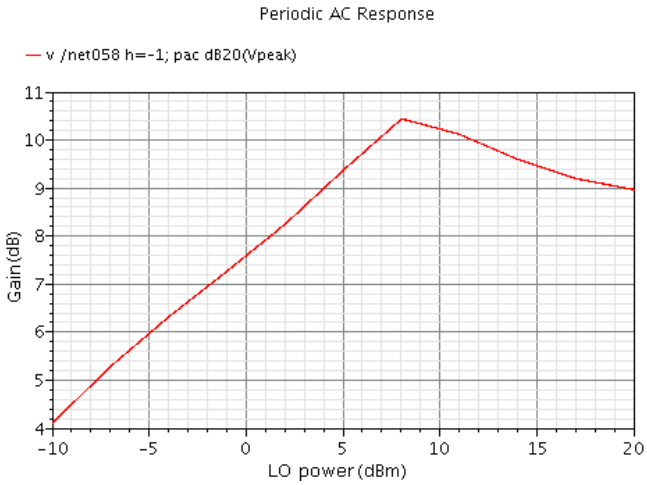


Fig. 5 – The conversion gain versus LO power.

Figure 6 is the 1 dB compression point of the proposed mixer, and the 1 dB compression point of the mixer is 10.32 dBm. Figure 7 is input third-order intercept point (IIP3) of the proposed mixer, and the IIP3 of the mixer is about 2.66 dBm. Obviously, from Figs. 6 and 7, it is clear that the proposed mixer can achieve relatively high linearity.

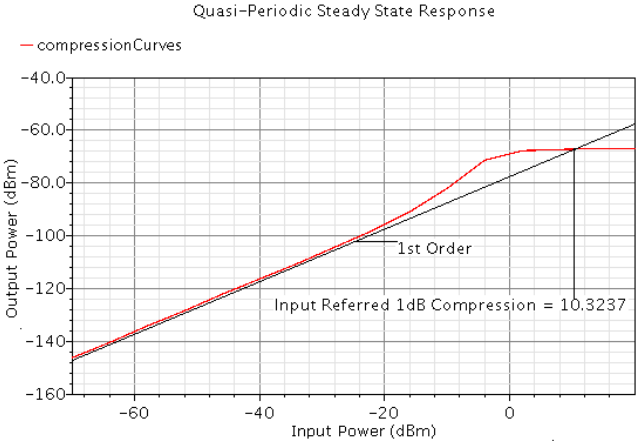


Fig. 6 – The 1 dB compression point of the mixer.

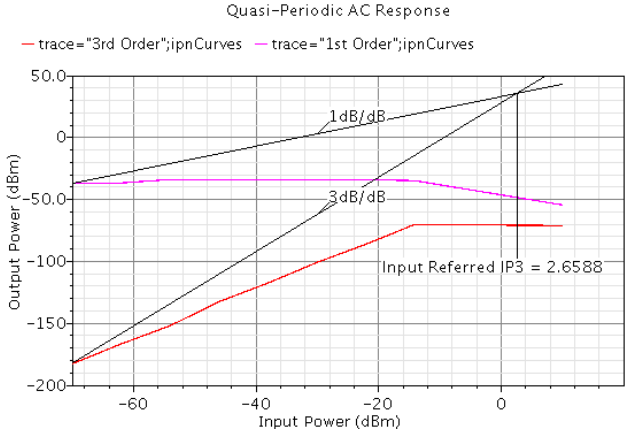


Fig. 7 – The IIP3 of the mixer.

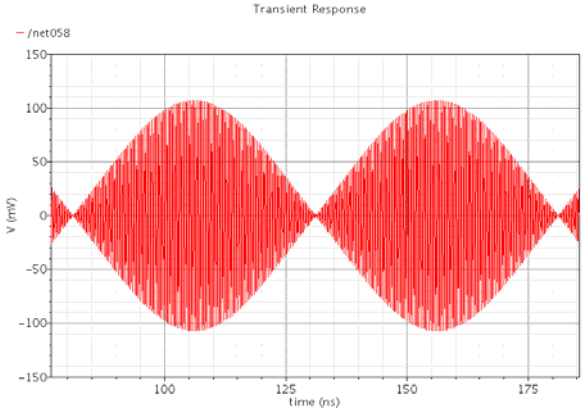


Fig. 8 – The transient analysis of the proposed mixer.

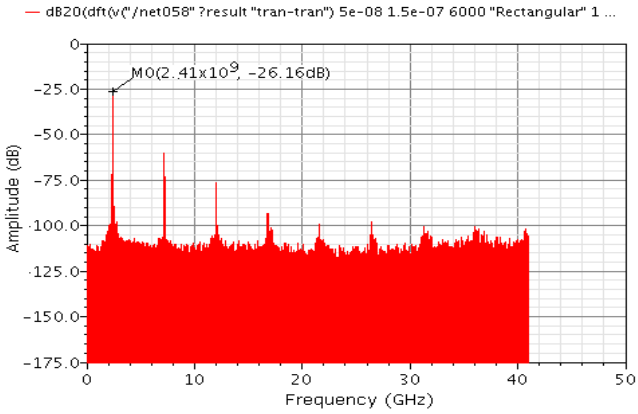


Fig. 9 – The simulated output spectrum of the proposed mixer.

Figure 8 is transient analysis of the proposed mixer. The input IF signal is chosen as 10 MHz, and its signal level is −25 dBm; the input LO signal is 2.4 GHz, and its signal level is 0 dBm. The signal in Fig.8 is the output RF signal ($V_{RF} = V_{RF+} - V_{RF-}$), and its frequency is 2.41 GHz. Figure 9 is the spectrum of the output RF signal, and it is clear that the output power of the mixer is concentrated at 2.41 GHz, and the other interference signals are relatively smaller.

The layout of the proposed mixer is presented in Fig. 10, which takes a compact chip area of 0.5 × 0.6 mm^2 including the testing pads.

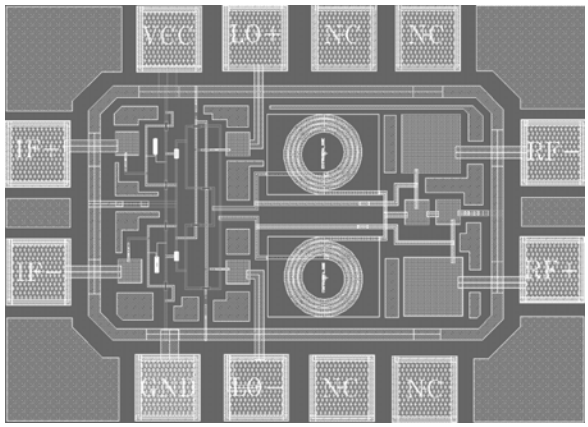


Fig. 10 – The layout of the proposed mixer (0.5 × 0.6 mm^2).

The comparison of the proposed mixer with other reported works are represented in Table 1. From the comparison table, we can know that the proposed mixer has the advantages of lower supply voltage, lower power consumption, higher linearity and smaller chip area than most of the other reported works.

Table 1

Performance comparison

References	[4]	[5]	[6]	[8]	[9]	[10]	This work
Technology (μm)	0.8	0.18	0.18	0.35	0.18	0.18	0.18
Supply voltage (V)	2.7	1.8	1.2	2.7	1.2	1.0	1.0
Power consumption (mW)	40.5	35	4.6	5.4	6	3.2	0.25
Conversion gain(dB)	2.9	15	7.1	14.6	7.1	11.9	10.5
LO Power (dBm)	-3.7	3	2	-10	5	0	0
1 dB compression point	-3.5	0	~	~	~	~	10.32
IIP3 (dBm)	-8.8	0.5	7.3	2	11.3	-3	2.66
Area (mm^2)	0.39	1.54	0.403	~	0.49	0.32	0.30

4.**CONCLUSIONS**

This paper presents a new CMOS low power up-conversion mixer based on Chartered 0.18 μm RF CMOS technology for 2.4 GHz WSN application. The current-reuse current-mirror and current-bleeding technique are used in the driver and switching stages of the mixer, which significantly decrease the supply voltage and power consumption, and improve the linearity of the mixer. The proposed mixer can work properly at 1 V supply voltage wih 0.25 mW power consumption. The proposed up-conversion mixer achieves high 1dB compression point and IIP3 at 10.32 dBm and 2.66 dBm with a large conversion gain of 10.5 dB.

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