RESISTORLESS CURRENT-MODE QUADRATURE OSCILLATOR WITH GROUNDED CAPACITORS

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Key words: Current mode, Quadrature oscillator, Current differencing transconductance amplifiers.

This paper presents a new Current Differencing Transconductance Amplifiers (CDTA)-based resistorless current-mode Quadrature Oscillator (QO). The proposed QO consist of two CDTAs and two grounded capacitors, and it is completely resistorless, which are suitable for monolithic integration. The QO can provide two explicit quadrature outputs at high impedance terminals, which are convenient for cascade. The oscillation frequency of the QO can be tuned from 46.63 MHz to 54.72 MHz by changing the control voltage, and the phase noise of the QO is –89.81dBc/Hz at 1 MHz offset. Moreover, all the active and passive sensitivities are low.

1. INTRODUCTION

As the important building blocks in analog signal processing systems, the quadrature oscillators and filters are drawing more and more attention in modern analog circuit design [1–2]. Quadrature oscillator is widely used in quadrature mixers, single-sideband modulators and all kinds of communication systems. The realizations of osillator using a variety of active elements have been reported [3–5]. In 2003, D. Biolek proposed the current differencing transconductance amplifier [6], which is a really current-mode element whose input and output are current form, and it is suitable for current mode circuit design. The CDTA-based oscillators are also reported in [7–15]. However, the works in [7–10] can not provide variable oscillation frequency, which can not be used as variable frequency oscillator; the works in [11–13] suffer from floating capacitors, and the work in [8–9, 13–14] use resistors, and they are not suitable for monolithic integration. The work reported in [15] realized three QOs using two CDTAs and two grounded capacitors, their structures are relatively simple, and the parasitic resistances at the input ports of the CDTAs used in [15] can be electronically adjusted. However, the

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CCCDTA just only suitable for the BJT technology. If the CMOS technology is used in [15], it has to use a floating resistor at the p terminal of the CDTA, because the parasitic resistance at the input terminals are relatively small [16], and the controllability of the bias current on the parasitic resistance will be reduced greatly.

In this paper, a new CDTA-based resistor-less current-mode QO with only two grounded capacitors is presented. The circuit only consists of two active and two passive elements, and the two passive elements used in the proposed QO are all grounded, and it is completely resistor-less, which is easy for monolithic integration. The QO can provide two explicit quadrature outputs at high impedance terminals, which are convenient for cascade. The oscillation frequency of the QO can be tuned from 46.63MHz to 54.72 MHz by changing the control voltage, and the QO can be used as variable frequency oscillator.

2. **THEORY AND PRINCIPLE**

2.1. CURRENT DIFFERENCING TRANSCONDUCTANCE AMPLIFIER

Fig. 1 is the symbol and ideal model of CDTA; Fig. 1 (a) shows the symbol of CDTA, and Fig. 1 (b) is the equivalent circuit of the CDTA. Equation (1) presents the terminal relation of the CDTA [8].

$$\begin{aligned} v_p &= v_n = 0 \\ i_z &= i_p - i_n \\ i_x &= g_m v_z = g_m Z_z i_z . \end{aligned} \tag{1}$$

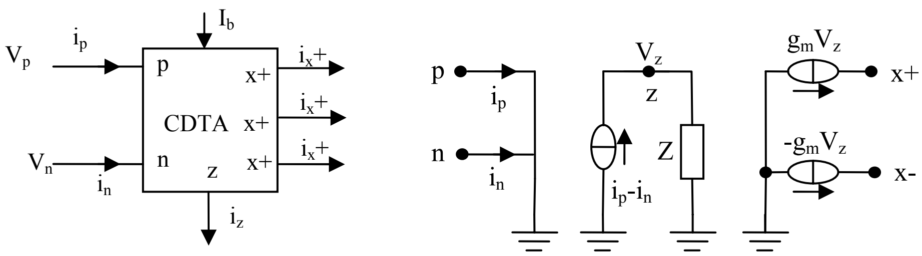

Fig. 1 – Symbol and ideal model of CDTA.

Figure 2 is the CMOS CDTA used in this paper, and it is derived from [10]. In order to use the current from terminal Z, an auxiliary Zc terminal is added in Fig. 2 to copy the current through terminal Z [17].

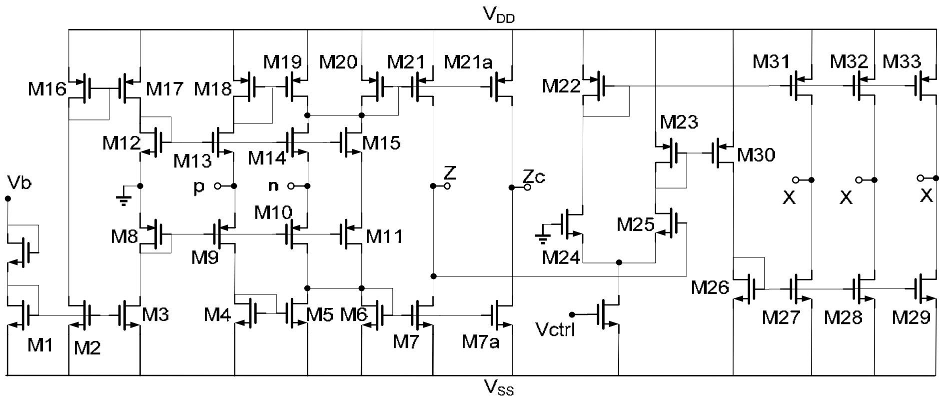

Fig. 2 – The CDTA used in this work.

2.2. THE PROPOSED CURRENT MODE QUADRATURE OSCILLATOR

The proposed QO is shown in Fig. 3, which employs only one CDTA, one resistor and two grounded capacitors.

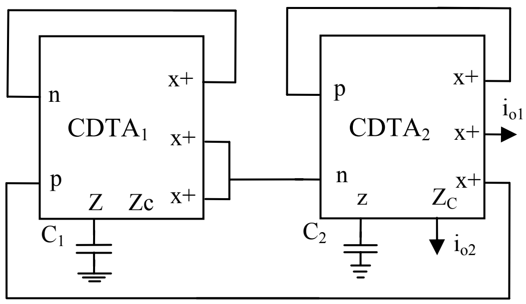

Fig. 3 –The proposed current-mode quadrature oscillator.

A routine circuit analysis using equation (1), we can get the characteristic equation of the QO is:

$$s^2 C_1 C_2 + s\left(g_{m1} C_2 - g_{m2} C_1\right) + g_{m1} g_{m2} = 0\,, \tag{2}$$

where g_{m1} and g_{m2} are the transconductance of the CDTA_1 and CDTA_2, respectively.

The proposed circuit has multiple inputs and multiple outputs, and it is necessary to discuss the stability of MIMO systems.

From equation (2), we can get the Hurwitz matrix as:

$$\Delta = \begin{bmatrix} g_{m1}C_2 - g_{m2}C_1 & 0 \\ C_1C_2 & g_{m1}g_{m2} \end{bmatrix}. \tag{3}$$

According to the Routh-Hurwitz stability criterion, the stable condition of the QO can be expressed as:

$$\begin{cases} C_1C_2 > 0 \\ g_{m1}C_2 - g_{m2}C_1 > 0 \\ g_{m1}g_{m2}\left(g_{m1}C_2 - g_{m2}C_1\right) > 0. \end{cases} \tag{4}$$

From equation (4), it is clear that $C_1C_2 > 0$ and $g_{m1}g_{m2} > 0$, and the stable condition of the QO is:

$$g_{m1}C_2 - g_{m2}C_1 > 0\,. \tag{5}$$

Actually, this is also the start-up condition of the QO (the loop-gain is a little greater than unity). When the oscillator gradually reaches the steady state, the frequency of oscillation (FO) can be approximately expressed as:

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}\,. \tag{6}$$

From Fig.3, the current transfer function between i_{o1} and i_{o2} is:

$$\frac{i_{o1}(s)}{i_{o2}(s)} = \frac{g_{m2}}{sC_2} = \frac{i_{o1}(\mathrm{j}\omega)}{i_{o2}(\mathrm{j}\omega)} = \frac{g_{m2}}{\omega C_2}e^{-\mathrm{j}90^{\circ}}\,. \tag{7}$$

So, the phase difference between i_{o1} and i_{o2} is 90°, and the two currents are quadrature, and the active and passive sensitivities of the oscillator are low, which can be expressed as:

$$S^{\omega_o}_{g_{m1},g_{m2}} = \frac{1}{2}, \quad S^{\omega_o}_{C_1,C_2} = -\frac{1}{2}\,. \tag{8}$$

3. NON-IDEAL ANALYSIS

Taking the tracking errors of the CDTA into account, the port relations of the non-ideal CDTA can be rewritten as:

$$\begin{aligned} & v_p = v_n = 0 \\ & i_z = \alpha_p i_p - \alpha_n i_n\,, \\ & i_x = \beta g_m v_z. \end{aligned} \tag{9}$$

where $\alpha_p = 1 - \varepsilon_p$ denotes the current tracking error from terminal p to z, $\alpha_n = 1 - \varepsilon_n$ denotes the current tracking error from terminal n to z, and β is transconductance inaccuracy factor from the z to x terminals of the CDTA, respectively.

The parasitic resistances and capacitances appear at high-impedance z and x terminals of the CDTA are ground. The parasitic capacitances at z terminals can be absorbed into the external capacitance C_1 and C_2, as they appear in shunt with them. The operating frequency should be chosen as $\omega_{osc} > \max[1/(C_1+C_{z1})R_{z1}, 1/(C_2+C_{z2})R_{z2}]$ to alleviate the effects of the parasitic capacitances and resistances.

Considering the tracking errors and taking the parasitics into account, the CO and FO of the proposed QO get modified and are given as:

$$g_{m1}C_2' + G_z\left(C_1' + C_2'\right) > \alpha_{p2}\beta_2 g_{m2}C_1', \tag{10}$$

$$\omega_o = \sqrt{\frac{\left(2\alpha_{n2}\beta_1 - \alpha_{p2}\right)\beta_2 g_{m1}g_{m2} + \left(G_Z + g_{m1} - \alpha_{p2}\beta_2 g_{m2}\right)G_Z}{C_1'C_2'}}, \tag{11}$$

where α_{pi}, α_{ni} and β_i are the parameters α_p, α_n and β of the i^{th} CDTA, $G_z = 1/R_{z1} = 1/R_{z2}$, $C_1' = (C_1+C_{z1})$, $C_2' = (C_1+C_{z2})$, respectively.

It can be seen from equation (10) and (11) that the parameters α_p, α_n, β and R_z will effect both the CO and FO of the QO. These parameters are the intrinsic resistances and stray capacitances of the CDTA, and they are dependent on temperature variations. So, these errors affect the sensitivity to temperature and the high frequency response of the QO, the CDTA should be carefully designed to minimize these errors. Considering this fact and make it possible in practice, these deviations are very small and can be ignored in theory.

4. **POST-LAYOUT SIMULATION RESULTS**

The performance of proposed circuits is verified using Cadence IC Design Tools 5.1.41 Spectre simulator with standard Charted 0.18μm CMOS technology. The chip layout design strictly obeys the Chartered Design Rule (YI-093-DR001_Rev1V_1.8 V-3.3 V) and Chartered Spice Model spec (yi093dr001_1v_00_20090731a), and it is designed as symmetrically as possible to minimize the mismatch in the signal paths. In the post-layout simulation, the supply voltage is ±1.8 V, the bias voltages $V_b = 1.2$ V, $V_{ctrl} = -0.7$ V, the capacitors $C_1 = 19$ pF, $C_2 = 21$ pF.

Figure 4 shows the post-layout simulation results of V_{o1} and V_{o2} during initial state with 100 Ω load resistors. From Fig. 4, it is clear that the starting time of QO is about 2.5 μs. Fig. 5 is the quadrature V_{o1} and V_{o2} from 5.0 μs to 5.1μs. From the markers M_0 and M_2 in Fig. 5, it is clear that the period of the QO is about 0.018 μs, and the frequency is about 55.5 MHz; from the markers M_0 and M_1, we can know that the phase difference between V_{o1} and V_{o2} is about 87°, and the two output signals are almost quadrature.

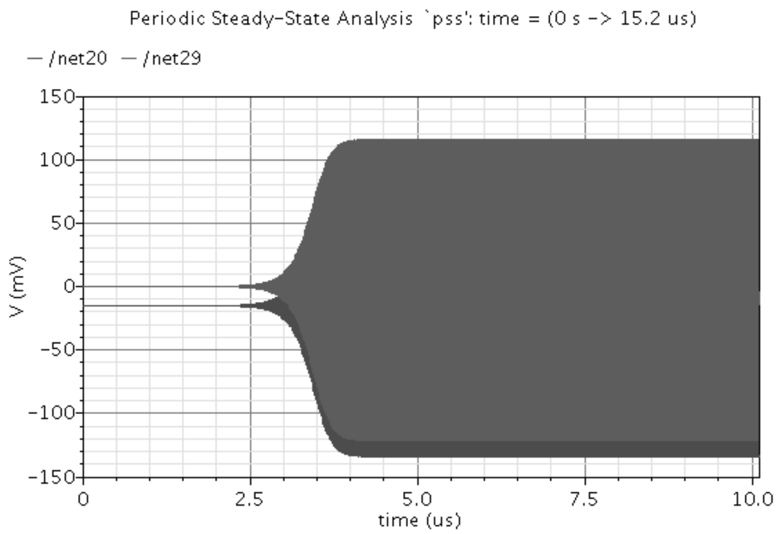

Fig. 4 – The simulated V_{o1} and V_{o2} during initial state.

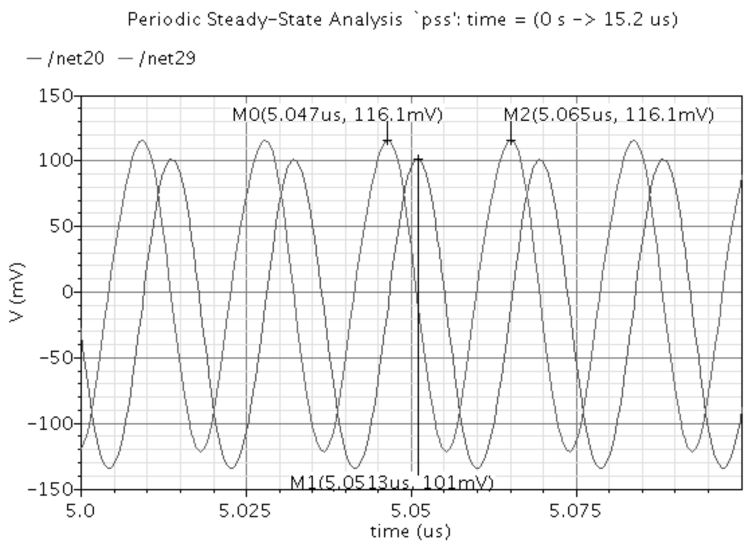

Fig. 5 – The quadrature outputs of V_{o1} and V_{o2} with 100Ω load resistors.

Figure 6 is the harmonic balance post-layout simulation result of V_{o1}. As is shown in Fig. 6 that the output power of V_{o1} is concentrated at in 55.5 MHz, and its magnitude is about – 9dBm (dBm is an abbreviation for the power ratio in decibels (dB) of the measured power referenced to one milliwatt (mW)). The output power of the other harmonic signals are relatively smaller.

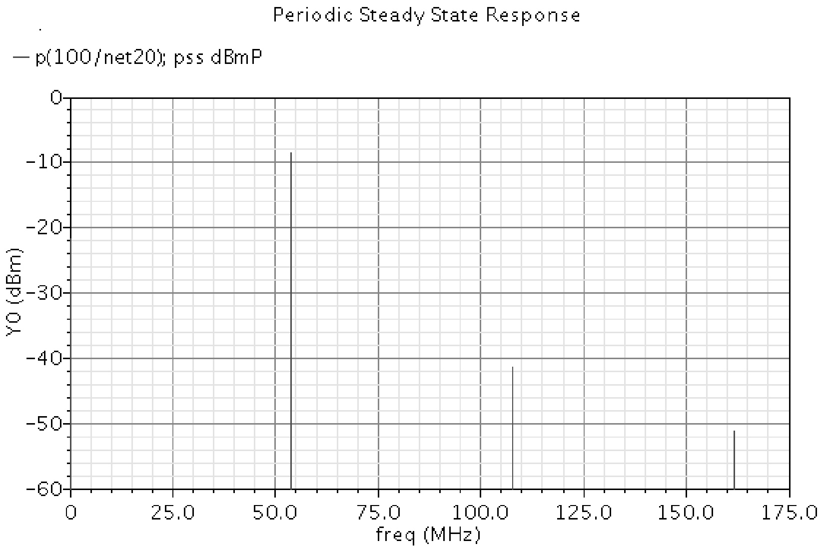

Fig. 6 – The harmonic balance simulation result of V_{o1}.

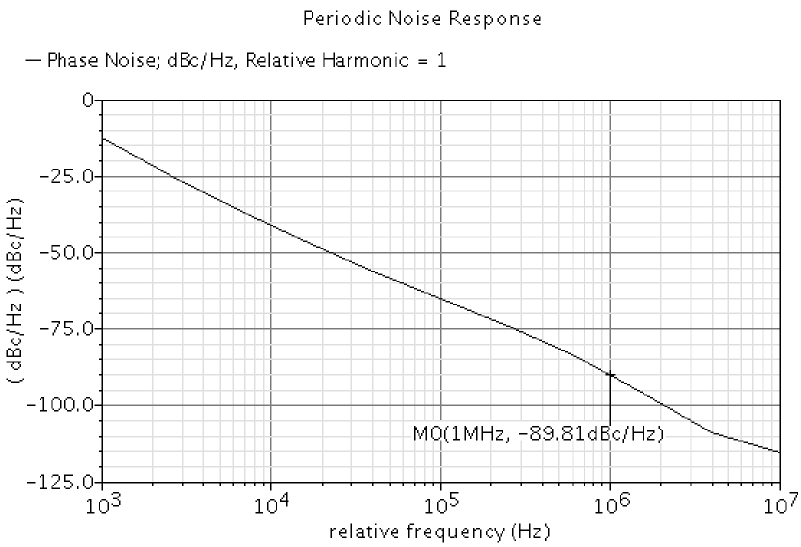

Fig. 7 – The phase noise of the QO.

Noise is a major concern in oscillators, because introducing even small noise into an oscillator leads to dramatic changes in its frequency spectrum and timing properties. This phenomenon, peculiar to oscillators, is known as phase noise [18], and their corresponding unit of measurement is (dBc/Hz). dBc (decibels relative to the carrier) is the power ratio of a signal to a carrier signal, expressed in decibels. For example, phase noise is expressed in dBc/Hz at a given frequency offset from the carrier. Figure 7 shows the phase noise of the QO, and the phase noise of the QO at 1 MHz offset is – 89.81 dBc/Hz while the carrier is 55.5 MHz.

Figure 8 is the output frequency versus the control voltage of the QO. As is shown in Fig. 8 that when the control voltage changing from – 0.9 V to – 0.55 V, the output frequency of the QO can be tuned from 46.63 MHz to 54.72 MHz, and the frequency tuning range is about 8.1 MHz. This makes the QO can be used as variable frequency oscillator.

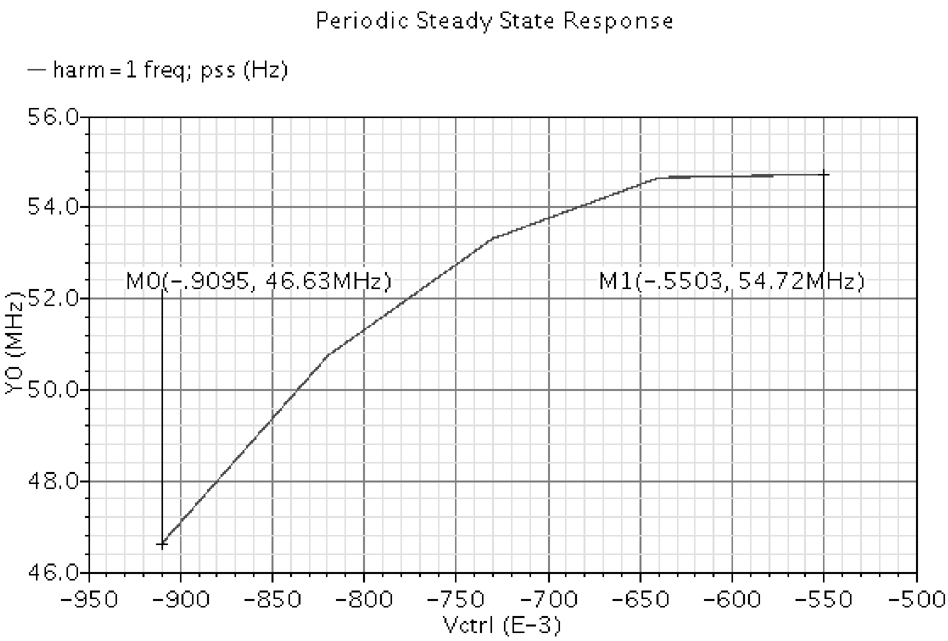

Fig. 8 – The output frequency versus the control voltage of the QO.

The layout diagram of the proposed QO is presented in Fig. 9. Because there is no inductance used in the QO, and it only takes a compact chip area of 0.47×0.33 mm^2 including the testing pads.

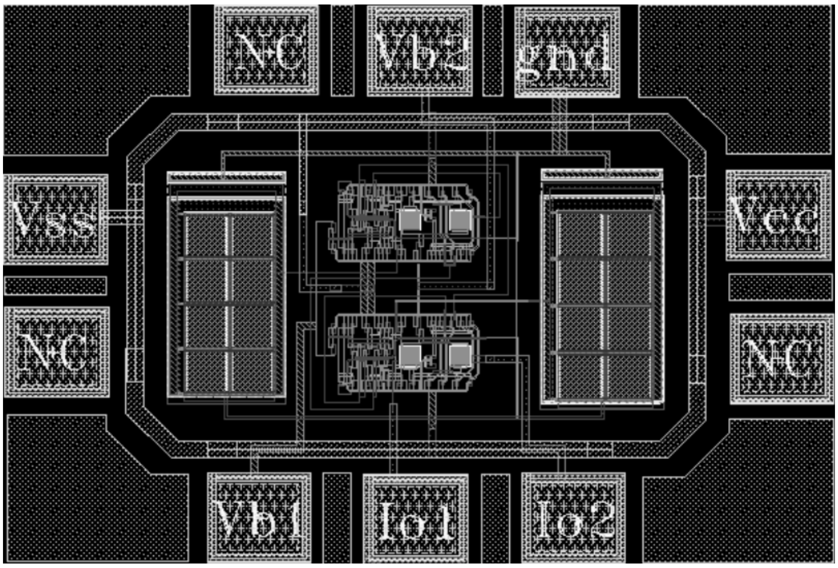

Fig. 9 – The layout of the proposed QO ($0.47 \times 0.33\text{mm}^2$).

5. **CONCLUSIONS**

A CDTA-based resistor-less current-mode QO with only two grounded capacitors is proposed in this paper. The proposed QO has following advantages: (a) It only consists of two CDTAs and two grounded capacitors, and it is easy for monolithic integration; (b) The QO can provide two explicit quadrature outputs at high impedance terminals, which are convenient for cascade; (c) The oscillation frequency of the QO can be tuned from 46.63 MHz to 54.72 MHz by changing the control voltage, and it can be used as variable frequency oscillator.

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