SETTLING-TIME-ORIENTED DESIGN PROCEDURE FOR TWO-STAGE AMPLIFIERS WITH CURRENT-BUFFER MILLER COMPENSATION

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A novel design procedure for two-stage operational amplifiers (op-amps) with current-buffer Miller compensation (CBMC) is proposed. The method is based on equations which relate both bias current and aspect ratio of transistors to the main amplifier parameters. The important innovation of the procedure is the definition of a systematic strategy to achieve the desired settling time by performing the op-amp dynamic behaviour optimization, which is badly needed in high-performance discrete-time applications. To prove the effectiveness of the proposed approach, a design example of a CBMC op-amp in 0.35 μm CMOS technology is presented.

1. **INTRODUCTION**

Two-stage operational amplifier (op-amp) configurations are widely employed, because they allow a suitable trade-off among the dc gain, speed, and output swing characteristics. As is known, an opportune frequency compensation network is required to guarantee the closed-loop stability in two-stage topologies. The current-buffer Miller compensation (CBMC) technique is one of the most popular approaches, owing to its benefits with respect to the other compensation schemes [1-3]. Design procedures for CBMC amplifiers were presented in the past 0[4, 5]. One of the most important objectives of the approaches in [4, 5] is the gain-bandwidth-product (GBW) enhancement by means of opportune choices of the op-amp parameters. However, owing to the third-order settling behaviour of CBMC op-amps [2, 3, 5] the GBW maximization does not correspond to the settling time minimization for the desired output response accuracy level [6, 7]. Unfortunately, the settling performance optimization is instead an essential aspect in designing op-

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amps for discrete-time applications such as switched-capacitor (SC) circuits, above all in order to avoid system power wasting [6]. Therefore, an ad-hoc approach has to be identified when the amplifier settling time is one of the main design concerns.

To the best of the authors' knowledge, a complete settling-time-based design procedure for CBMC op-amps is not available in the literature. Actually, a systematic criterion to reach the optimization of the CBMC amplifier settling performances by properly sizing the compensation network has recently been presented in [7]. As demonstrated by the exhaustive analysis reported in [7], this criterion allows significant improvements on the op-amp settling-time/power-consumption ratio with respect to conventional GBW-oriented approaches, even in the presence of parametric variations.

Starting from the settling time minimization strategy in [7], a complete design procedure for CBMC op-amps is presented in this paper. The proposed approach is based on well-defined rules which relate the bias current and the aspect ratio of each transistor to the main amplifier parameters, developed to take also settling time specification into account. Before entering into details of the design methodology, a set of rules to control the amplifier speed performances is introduced in Section 2. The design procedure is then presented in Section 3 and applied to the design of a CBMC op-amp in 0.35 μm CMOS technology, in Section 4. Finally, some conclusions are reported in Section 5.

2. **DESIGN RULES FOR CBMC SPEED PERFORMANCES**

The typical fully-differential two-stage CBMC op-amp is depicted in Fig. 1. MOSFETs M1-M5 and M6-M7/M8-M9 implement the differential and the common-source stages, respectively. M10-M11 implement the current buffers which are biased by the current I_b. C_C is the compensation capacitor and C_0, C_L are the total lumped output capacitances to be driven by the first and the second stage, respectively.

The closed-loop speed performances of the amplifier depend on both slewing and linear settling characteristics. The former can be roughly imposed by exploiting quite simple early-design rules. As a first-order approximation, the op-amp slew rate (SR) is indeed determined by the minimum between the first (SR_1) and second stage (SR_2) slew rates, which are simply expressed as follows [8]:

$$\mathrm{SR}_1 = \frac{2I_{1,2}}{C_C}, \tag{1}$$

$$\mathrm{SR}_2 = \frac{2I_{7,9}}{C_C + C_L}, \tag{2}$$

where $I_{1,2}$ and $I_{7,9}$ are the bias currents of $M_{1,2}$ and $M_{7,9}$, respectively.

Instead, the linear settling characteristics are related to the amplifier parameters according to a more complex relationship. In fact, the closed-loop behaviour of the amplifier in Fig. 1 is well-described by the following third-order transfer function [2, 7]:

$$G(s)=\frac{G_0\left(1+\frac{C_C}{g_{mb}}s\right)}{1+\frac{C_C}{f}\left(\frac{1}{g_{m1,2}}+\frac{f}{g_{mb}}\right)s+\frac{C_0}{fg_{m1,2}g_{m7,9}}(C_C+C_L)s^2+\frac{C_CC_0C_L}{fg_{m1,2}g_{m7,9}g_{mb}}s^3}. \quad (3)$$

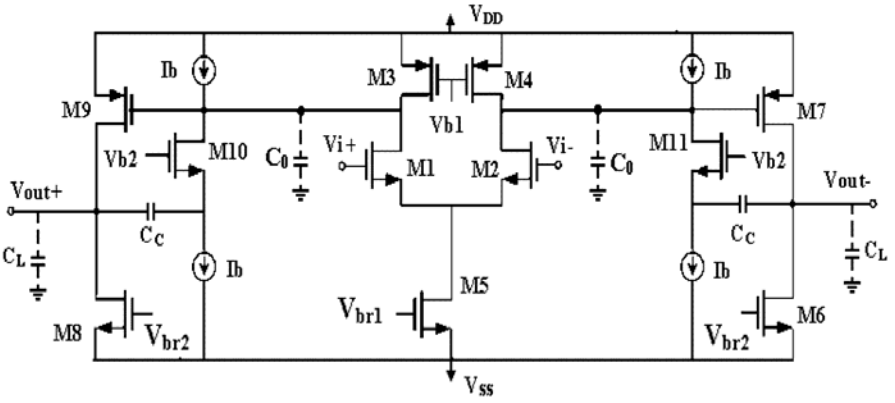

Fig. 1 – Fully differential two-stage amplifier with current-buffer Miller compensation.

In (3), $g_{m1,2}$, $g_{m7,9}$ and g_{mb} are the transconductances of $M_{1,2}$, $M_{7,9}$ and $M_{10,11}$, respectively, f is the feedback factor which models the feedback network in typical applications, and G_0 is the closed-loop dc gain. The transfer function (3) has, in general, one real pole p_1, two complex-poles characterized by a natural frequency ω_n and a damping factor ζ, and one LHP zero z_1. As discussed in [7], a systematic strategy for the settling performances optimization of (3) can be identified by introducing the normalized time $T=\zeta\omega_n t$, $\zeta\omega_n$ and t being the real part of the closed-loop complex poles and the time variable, respectively. By indicating with $\rho=\frac{p_1}{\zeta\omega_n}$ the normalized real pole, t_S and $T_S=\zeta\omega_n t_S$ the absolute and the normalized linear settling times, respectively, the following expressions for t_S, C_C and g_{mb} arise under the typically verified hypothesis that C_C is sufficiently smaller than C_L [7]:

$$t_S = \frac{T_S}{\zeta\sqrt{\left(1+\frac{2}{\rho}\right)}}\sqrt{\frac{C_0 C_L}{f g_{m1,2} g_{m7,9}}}\,, \tag{4}$$

$$C_C = \frac{2(1+2\rho\zeta^2+\rho^2\zeta^2)}{(\rho+2)\zeta}\sqrt{\frac{f}{\rho(\rho+2)}\frac{g_{m1,2}}{g_{m7,9}}C_0 C_L}\,, \tag{5}$$

$$g_{mb} = 2f\left(\frac{1+2\rho\zeta^2+\rho^2\zeta^2}{\rho}\right)g_{m1,2}\,. \tag{6}$$

The settling performance optimization is carried out by performing numerical simulations to determine the values of ρ and ζ which minimize T_S for the desired output response accuracy level [7]. Thus, (4)–(6) can be profitably used to size the two op-amp stages and the compensation network in order to reach the desired linear settling time by means of an optimized dynamics.

3. **PROPOSED DESIGN PROCEDURE**

The design procedure will be developed by taking the specifications on the noise, the linear settling time, the slew rate, the input common range and the output swing into account. Other amplifier characteristics such as the dc gain, the power-supply and the common-mode rejection ratios are extremely difficult to predict by calculations, because of their strong dependence on the transistor output resistances. Therefore, they can be evaluated only by performing circuit simulations based on complex transistor models and cannot be simply included in an early-design procedure [4]. To fix both the aspect ratio and the bias current of the transistors, the following first-order relationships among the transconductance g_{mn}, the aspect ratio $\frac{W_n}{L_n}$, the drain current I_n, the process transconductance K_n and the saturation voltage V_{DSATn} of a generic MOSFET M_n in the saturation region will be exploited:

$$\frac{W_n}{L_n} = \frac{g_{mn}{}^2}{2K_n I_n}\,, \tag{7}$$

$$V_{DSATn} = \sqrt{\frac{2L_n I_n}{K_n W_n}} \,. \tag{8}$$

The proposed methodology starts from the noise specification. The contribution of the flicker (1/*f*) noise at low frequencies, which can be anyway reduced by using large input devices, will be neglected in the procedure [4], thus only the thermal noise is considered. The following equation relates the transconductances of the amplifier first-stage transistors to the thermal noise [4]:

$$E^2{}_n(f) = \frac{16}{3}\frac{KT}{g_{m1,2}}\left(1+\frac{g_{m3,4}}{g_{m1,2}}\right), \tag{9}$$

where $E^2{}_n(f)$, $g_{m3,4}$, K and T are the input-referred thermal noise power spectral density, the transconductance of MOSFETs $M_{3,4}$, the Boltzmann constant and the absolute temperature, respectively. Equation (9) univocally fixes the value of $g_{m1,2}$ on the basis of the required value of $E^2{}_n(f)$ when $g_{m3,4}$ is neglected 0[4] or is chosen as an assigned fraction h (h<1) of $g_{m1,2}$, for the sake of simplicity:

$$g_{m1,2} = \frac{16}{3}\frac{KT}{E^2{}_n(f)}(1+h). \tag{10}$$

Once $g_{m1,2}$ is determined, $g_{m7,9}$ is set on the basis of the required linear settling time. In fact, the following relationship arises from (4):

$$g_{m7,9} = \left(\frac{T_S}{t_S\zeta}\right)^2 \frac{1}{\left(1+\frac{2}{\rho}\right)}\frac{C_0 C_L}{f g_{m1,2}} \,. \tag{11}$$

Starting from the chosen values for $g_{m1,2}$ and $g_{m7,9}$, the compensation network is then sized according to (5) and (6). It is clear that the parasitic capacitances of amplifier transistors determine the value of C_0. Moreover, they also affect the values of C_L and f. Since the parasitics are unknown in the early-design phase, reasonable estimations for C_0, C_L and f, have to be used in (5), (6) and (11) to carry out a first evaluation for C_C, g_{mb} and $g_{m7,9}$. If needed, the latter parameters can then be properly adjusted after a first sizing of op-amp transistors, by considering the actual parasitic capacitance values resulting from circuit simulations. The bias currents of $M_{1,2}$ and $M_{7,9}$ are chosen from (1) and (2) to meet the slew rate requirement. As a first choice, $SR_1 = SR_2$ can be set. The aspect ratios of $M_{1,2}$, $M_{3,4}$ and $M_{7,9}$ are then determined according to (7).

To complete the procedure, the specifications on the output swing and the common mode input range are also contemplated. The single-ended positive (OSW^+) and negative (OSW^-) output swings are given by:

$$OSW^+ = V_{DD} - \left|V_{DSAT7,9}\right| , \tag{12}$$

$$OSW^- = V_{SS} + V_{DSAT6,8} . \tag{13}$$

respectively. According to (7) and (8), $V_{DSAT7,9}$ is not an independent parameter when $I_{7,9}$ and $g_{m7,9}$ are already set to meet the slew rate and linear settling requirements. This means that if the constraint on the positive output swing (12) is not satisfied, the values of $I_{7,9}$ and $g_{m7,9}$ have to be opportunely recalculated. Equations (8) and (13) are instead used to determine the aspect ratio of the NMOS $M_{6,8}$. The negative (CMR^-) and positive (CMR^+) common-mode input voltages are:

$$CMR^- = V_{SS} + V_{DSAT1,2} + V_{TN} + V_{DSAT5} , \tag{14}$$

$$CMR^+ = V_{DD} - \left|V_{DS3,4}\right| + V_{TN} , \tag{15}$$

where $V_{DS3,4}$ and V_{TN} are the drain-source voltage of $M_{3,4}$ and the NMOS threshold voltage, respectively. From (8) and (14), M_5 is sized on the basis of the required value of V_{DSAT5}, $V_{DSAT1,2}$ being fixed by $I_{1,2}$ and $g_{m1,2}$. The value of $V_{DS3,4}$ in (15) is instead determined by the sizing of $M_{3,4}$, arising from the imposed value for $g_{m3,4}$. Moreover, $V_{DS3,4}$ cannot be easily predicted by calculations, as instead occurs in the single-ended amplifier configuration 0 [4]. As a consequence, if circuit simulations show that the specification on CMR^+ is not satisfied, the aspect ratio of $M_{3,4}$ has to be corrected and the above design steps have to be retraced.

As previously discussed, accurate circuit simulations are also inescapable in order to estimate the transistor channel lengths required to reach adequate output resistance values for the two amplifier stages. In this scenario, the proposed well-defined design procedure allows an aware and focused use of simulations, avoiding blind trial-and-error processes which can result in poor performances and excessive design time. The proposed design flow is summarized in Fig. 2.

4. **DESIGN EXAMPLE**

To prove the effectiveness of the proposed design approach, the CBMC op-amp in Fig. 1 was designed in a commercial 0.35 μm CMOS technology. The amplifier was employed in the unity-gain capacitive buffer of Fig. 3 [10]. In the

circuit, C_{IN} models the op-amp input capacitance and C_{EXT} represents the external load capacitance.

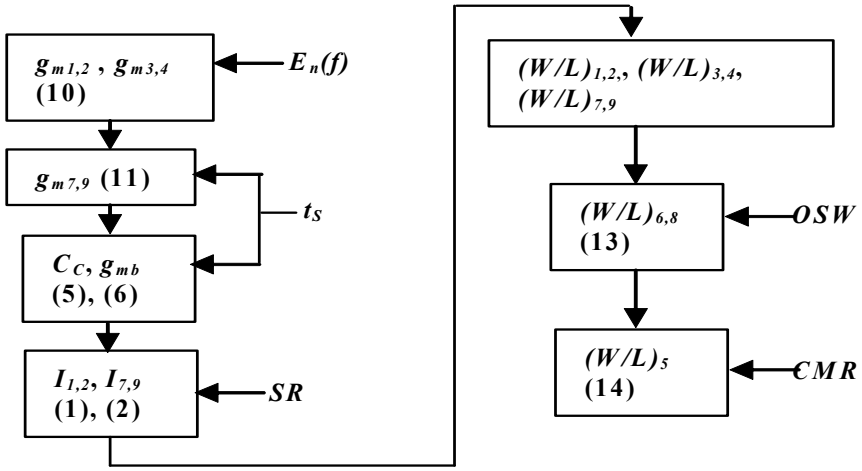

Fig. 2 – Proposed design flow.

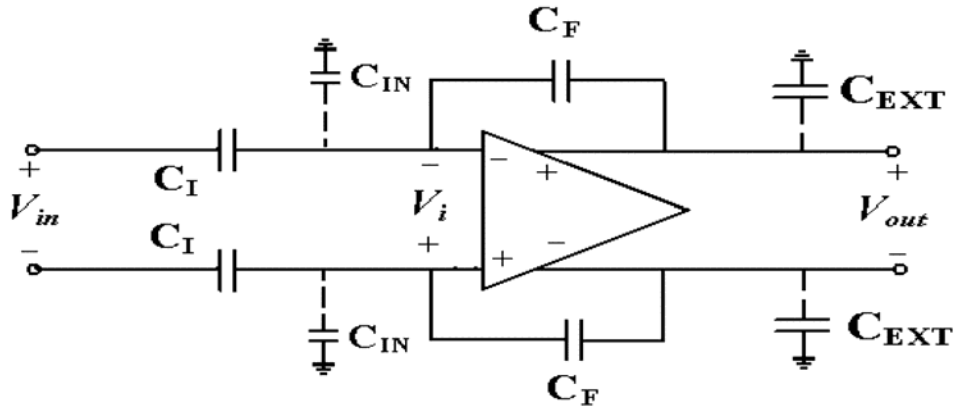

Fig. 3 – Unity-gain capacitive buffer.

In this case, the feedback factor f and the total op-amp output capacitance C_L are $f = \dfrac{C_F}{C_F + C_I + C_{IN}}$ and $C_L = C_{EXT} + \dfrac{C_F(C_I + C_{IN})}{C_F + C_I + C_{IN}}$, respectively [9].

C_I = 1 pF, C_F = 1 pF and C_{EXT} = 10 pF were assumed. The design was carried out to meet the specifications summarized in Table 1.

Table 1

Main amplifier parameters

Parameter	Specification	Simulated
DC gain	≥ 80 dB	80 dB
t_S^+ / t_S^- (0.1% Accuracy level)	15 ns	14.8 ns
SR	60 V/μs	60 V/μs
$E_n(f)$ @ T = 300°K	$15nV/\sqrt{Hz}$	$14nV/\sqrt{Hz}$
$OSW=OSW^+-OSW^-$	>1.5 V	2 V
$CMR=CMR^+-CMR^-$	>1 V	1.1 V
GBW	–	58 MHz
Phase Margin	–	53 °
Power @ 3.3 V	–	4.8 mW

From numerical simulations 0 [7], ρ = 1.05, ζ = 0.73 and T_{SS} = 4.73 result, for a desired 0.1% output accuracy level. By exploiting the proposed procedure, the following values of the main amplifier parameters were obtained: $g_{m1,2}$ =150 μA/V, $g_{m3,4}$ = 50 μA/V, $g_{m7,9}$ = 1005μA/V, $I_{1,2}$ = 13 μA, $I_{7,9}$ = 360 μA, C_C = 0.35 pF and g_{mb} = 380 μA/V. The amplifier transistors are sized as summarized in Table 2.

Table 2

Amplifier MOSFET dimensions

MOSFET	$M_{1,2}$	$M_{3,4}$	M_5	$M_{6,8}$	$M_{7,9}$	$M_{10,11}$
W/L (μm)	7/1	10/4	15/2	50/2	25/0.5	5/0.35

The exact parasitic capacitor values, obtained from HSPICE circuit simulations, are C_0 = 0.088 pF and C_{IN} = 0.03 pF. Simulation results are reported in Table 1. As is noticeable, the positive/negative step 0.1% settling time is very close to the target value of 15 ns. The amplifier response for a 300 mV amplitude step is portrayed in Fig. 4. The above example has demonstrated the usefulness of the proposed design methodology in order to properly size both CBMC amplifier stages and compensation network when the time response optimization is one of the main concerns.

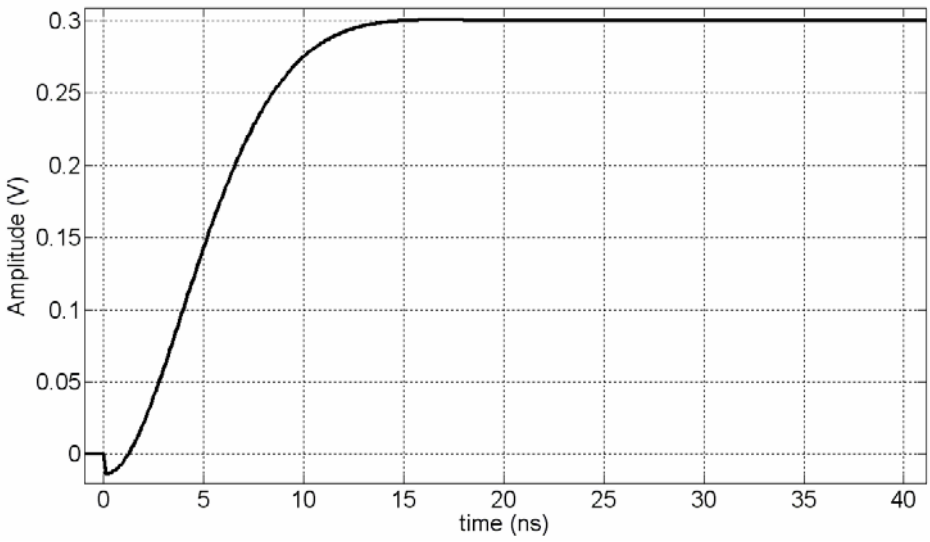

Fig. 4 – 300 mV-amplitude step response.

5. **CONCLUSIONS**

In this paper, a new complete design procedure based on the systematic settling performance optimization for two-stage CBMC op-amps has been developed. Straightforward rules have been defined in order to fix the bias current and the aspect ratio of op-amp transistors on the basis of the main design specifications. The effectiveness of the procedure has been proved by the design of a CBMC amplifier in 0.35 μm CMOS technology.

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