1. INTRODUCTION

Three-phase active and passive rectifiers are used frequently in applications such as high voltage dc systems, uninterruptable power supplies, variable speed drives, etc. Among all the existing rectifier structures, harmonic input current is of significant concern, since it leads to lower power quality and output voltage distortion. In addition, achieving unity power factor is challenging in the aforementioned structures. In order to overcome the existing problems in passive rectifiers, passive, active or hybrid filters are employed. The drawback of this solution is the increase of the system cost and loss leading to the reduction of the conversion efficiency. Active rectifiers are considered as an ultimate solution capable of achieving unity power factor and low input current total harmonic distortion (THD) [1]. So far, several structures of three-phase active rectifiers have been introduced, all presenting some advantages and disadvantages in various applications [2–5].

Nowadays, amongst three-phase active converters, Vienna rectifier, a unidirectional 3-level boost converter has been of increasing interest. Compared with the conventional active rectifiers, Vienna rectifier presents the following advantages: simple power stage and control structure, low electromagnetic interference (EMI), low voltage stress, low switching loss and low cost [6]. Therefore, it can be used in medium/high voltage applications such as telecommunication and wind energy conversion systems [1, 7–9]. Also, Vienna rectifier is regarded as one of the promising boost structures in power factor correction and input current harmonic reduction. The schematic diagram of Vienna rectifier is presented in Fig. 1.

Up to now, various switching methods and control techniques have been introduced in the literature for Vienna rectifier. These schemes are completely different from the conventional strategies used for three-phase rectifier structures.

Space vector modulation (SVM) control strategy for Vienna rectifier is developed in [10–12]. The voltage vector selection and calculation of the duration time are much more complicated than other strategies. The complexity and the computation burden are further increased due to the dependency of phase voltage to the input current direction.

In carrier-based pulse width modulation (CB-PWM) method reported in [10, 11], two carrier waves are employed to realize the pulse width modulation (PWM). Neutral point potential is also balanced by adding offset signals to the phase reference voltages, which leads to continuous switching method, known as continuous PWM. Reference voltage generation is much easier compared with SVM strategy. However, its practical implementation is complicated in terms of synchronization of two carrier waves with same frequencies. In [13], single-carrier wave PWM is realized to overcome the problem existing in CB-PWM, but still balancing dc link voltage remains a challenge. Hysteresis current controller in [14] has the merit of fast dynamic response and simple implementation allowing the usage of minimum hardware. However, the controller presents

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inherent disadvantage of variable switching frequency which is an issue in converter protection.

In [15], the virtual flux based direct power control for Vienna rectifier has been proposed. No need for the input voltage sensors, the current regulation loop and PWM voltage modulation block along with the active and reactive power decoupling are some of the salient advantages of this method.

However, due to the three-level nature of the Vienna configuration, balancing the output capacitors voltages is inevitable and an extra switching table has to be established to control the capacitors voltages. Furthermore, in this method, errors between the estimated instantaneous active and reactive powers with their reference values are passed through two hysteresis controllers which in turn, provides variable switching frequency. The requirement for high speed processor is also considered as another issue in this control method.

An optimal switching sequence model predictive control (OSS-MPC) strategy, based on SVPWM, is proposed for Vienna rectifier in [17]. Here, an improved OSS-MPC method is utilized to control the input currents. However, since the Vienna rectifier voltages depend on the polarity of the input currents, applying a proper switching sequence and voltage vectors are inevitable to obtain good current quality. The switching sequence with minimum cost function will be the optimal switching sequence. A proportional–integral (PI) controller is also designed to regulate the dc-link voltages.

Most of the continuous PWM strategies can considerably satisfy the control objectives of Vienna rectifier. However, in case of Vienna rectifier, with satisfactory operational characteristics in high power applications, applying discontinuous approaches can significantly decrease the switching loss [17–19]. Discontinuous PWM (DPWM) methods are advantageous with respect to efficiency, especially as reported in [17]. If the switching loss is not considered in a converter, high frequency strategies such as CB-PWM can be more effective in converter control. In return, when high efficiency is of the most importance, employing methods with lower switching loss seems practical [18]. In [17], SVM-based DPWM method is introduced within a limited range of modulation index. Implementation of DPWM method based on SVM seems complicated using low performance microcontroller units, while high performance is achieved in the expense of more cost. [19]. Developed a carrier based DPWM strategy for Vienna rectifier. In this method, dc link voltage balancing is realized through injection an offset to the phase reference voltages. This strategy offers simpler implementation than SVDPWM techniques. Yet, to satisfy the important regulation (IR) existing in Vienna rectifier, that is; the sign of the current should be the same as that of the input voltage, an additional offset calculation has to be performed to modify the reference voltage, while the offset injection range is varied according to the modulation index.

In Vienna rectifier, the neutral point is connected to the input inductors via semiconductor switches. Though, dc link voltage unbalance is the most challenging problem in converter control, since it results in high voltage stress on semiconductor devices and input current distortion. Hence, some considerations should be introduced to overcome the unbalance problem in the rectifier structure [20, 21]. In most conventional control strategies, an offset voltage injection or an extra feedback control loop including PI controller is modified to provide dc link voltage balancing in the expense of more cost and complexity of the whole system [22–24]. Another limitation existing in Vienna rectifier is the dependency of switching states to the direction of input current which results in current distortion at zero-crossing points. In order to overcome this problem, a modified SVM control strategy is proposed in [25, 26]. This target can be reached near the current zero-crossing point by clamping the related phase to zero. [27], presented a carrier-based discontinuous space-vector modulation (CB-D SVM) method with varying clamped area for Vienna rectifier in high switching frequency applications. The proposed CB-D SVM method can reduce terminal voltage errors by only clamping zero-crossing phase to neutral-point, and the proposed method with varying clamped area can reduce clamped area around zero-crossing and get lower input current THD. However, the aforementioned disadvantages of CBPWM and SVM are still existent.

In this paper, based on CLD concept, a novel discontinuous PWM method is introduced for Vienna rectifier. In the proposed method, Vienna rectifier is decoupled into two two-level separately controlled boost converters in every 60˚ region, in which the closed loop controller design can be simplified to the control of dc-dc converters. The proposed strategy also has the merit of using just one carrier-wave for modulation and offers lower switching loss which is an impressive issue in medium/high voltage applications.

In Section 2, the novel DPWM strategy based on circuit-level-decoupling concept is introduced for Vienna rectifier. dc link voltage variation is investigated in Section 3. In Section 4, the switching loss calculation has been conducted and compared for both conventional carrier based PWM and the proposed approach. Finally, the control strategy performance is validated via simulation on 1 kW and 10 kHz Vienna rectifier. The simulation results prove the effectiveness of the whole system configuration.

2. CIRCUIT-LEVEL DECOUPLING CONCEPT

Vienna rectifier structure consists of three semiconductor switches (S_a, S_b and S_c), low loss silicon carbide diodes and dc link capacitors (C_1 and C_2) as shown in Fig. 1. The rectifier voltages (V_{a_r}, V_{b_r} and V_{c_r}) are generated based on the switching pattern applied on S_a, S_b and S_c. Three-phase input voltages (V_{a_i}, V_{b_i} and V_{c_i}) are shown in Fig. 2.

In this paper, a discontinuous PWM method with the circuit-level decoupling concept has been proposed for Vienna rectifier, based on the existing strategy for three-level NPC inverters [28, 29]. According to the figure, each phase voltage can be divided into 6 regions per fundamental cycle. Inspecting three-phase voltages in each 60˚ region one common fact is that, there is a sign transition in one phase voltage while the sign of the other two voltages is remained unchanged. Considering this fact, the switch with transitional phase voltage is always turned on during the whole region,
Sb will be switched between dp < dn cycle; 1,2,4 for (switching sequences must be applied during each switching process of inductor voltages is presented below.

As seen in Fig. 3, in view of the fact that phase (a) voltage has transitional sign, the corresponding switch is kept on during the entire period. Since the voltage in phase (c) is positive during the whole region, Sc is switched between p and n. While, the voltage in phase (b) is always negative and Sb will be switched between N, n. Duty cycles for switches in phase (c) and (b) can be defined as dp and dn where 

\[ d_p = \frac{T_{bus}}{T}, \quad d_n = \frac{T_{bus}}{T}, \]  

(1)

which \( T_{bus}(i=c,b) \) is the on-time of each switch in region I.

According to Fig. 2, for the period (–30°~0°), the absolute value of phase (c) current is higher than that of phase (b) and thus, \( dp < dn \). The opposite is found during (0°~ 30°).

Regarding the relation between \( dp \) and \( dn \), two different switching sequences must be applied during each switching cycle; 1,2,4 for \( dp < dn \) and 1, 3, 4 for \( dp > dn \). The switching sequences and the resulting inductor voltages in region I are summarized in Table 1. To give a better illustration of the analysis carried out, the extraction process of inductor voltages is presented below.

Table 1

<table>
<thead>
<tr>
<th>Switching sequence</th>
<th>( S_b )</th>
<th>( S_c )</th>
<th>( V_{lc} )</th>
<th>( V_{lb} )</th>
<th>( V_{la} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>off</td>
<td>on</td>
<td>(- V_c)</td>
<td>(- V_b)</td>
<td>( V_a)</td>
</tr>
<tr>
<td>2</td>
<td>on</td>
<td>off</td>
<td>( V_c )</td>
<td>(- V_b)</td>
<td>(- V_a)</td>
</tr>
<tr>
<td>3</td>
<td>off</td>
<td>on</td>
<td>( V_c )</td>
<td>(- V_b)</td>
<td>(- V_a)</td>
</tr>
<tr>
<td>4</td>
<td>off</td>
<td>off</td>
<td>( V_c )</td>
<td>(- V_b)</td>
<td>(- V_a)</td>
</tr>
</tbody>
</table>

The same analysis has been extended to other switching states and regions, which are eliminated here to avoid tedious calculations.

Assignment of duty cycles \( (d_p, d_n \text{ and } d_t) \) along with the derivation of the modulation signals \( (Cont_p \text{ and } Cont_n) \) are listed in Table 2 for each region. \( d_t = 1 \) is allocated to the switch with on state during each region.

Considering the decoupled circuits in Fig. 4, KVL equations for switching state (2) are written as follow

\[-V_c + L_c \frac{dV_c}{dt} - L_a \frac{dV_a}{dt} + V_a + E = 0, \]

(2)

\[-V_c + L_a \frac{dV_c}{dt} - L_b \frac{dV_b}{dt} + V_b = 0. \]

(3)

Assuming the three-phase input voltages and currents to be symmetrical, the inductor voltages, are extracted for region I

\[ V_{la} = V_a + \frac{1}{3} E, \]

\[ V_{lb} = -V_b - \frac{1}{3} E, \]

\[ V_{lc} = V_c - \frac{2}{3} E. \]

(4)

Since the switching frequency is much higher than the line frequency, Vienna rectifier can be decoupled into two two-level de-dc boost converters during each region (Fig. 4).

Hence, applying volt-second balance to the inductors during a switching cycle, duty cycles of the switches will be met through the following formulas for region I

\[ \begin{align*}
V_c d_a + \left(V_c - \frac{1}{3} E\right) (d_p - d_n) + (V_c - E)(-d_p) &= 0 \\
V_b d_a + \left(V_b - \frac{2}{3} E\right) (d_p - d_n) + (V_b - E)(-d_p) &= 0 \\
V_c d_a + \left(V_c - \frac{1}{3} E\right) (d_p - d_n) + V_a (1 - d_p) &= 0 \\
\Rightarrow \left\{ \begin{array}{l}
\frac{d_p}{E} = \frac{E - (2V_a + V_c)}{E} \\
\frac{d_n}{E} = \frac{E - (V_c - 2V_b)}{E}
\end{array} \right.
\end{align*} \]

The implementation process of the proposed method is illustrated in Fig. 5, which is divided into 4 major blocks:

1. Region selector
2. Modulation signal selector (MSS)
3. PWM unit
4. Duty cycle allocator (DCA).

The active operating region is determined through
observation of the input reference voltages ($V_{abc}^*$) in region selector. $Cont_p$ and $Cont_n$ signals are derived from MSS block based on the active operating region number and the information listed in Table 2. The resulting modulation signals are then compared with carrier wave in PWM unit and the duty cycle signals $d_p$ and $d_n$ are obtained. The duty cycles are evaluated through applying a simple PWM technique on two boost converters modeled in each region.

These signals are then allocated to the switches $S_a, S_b$ and $S_c$ in DCS block, according to the information acquired from region selector. Therefore, taking into account the analysis conducted in Table 2, algorithm of the modulator is so simple, and the implementation will be more straightforward in comparison to the conventional methods such as SVPWM and CB-PWM.

Furthermore, based on the switching strategy, each phase is clamped to zero during zero-crossing point of the input current. Consequently, the previously mentioned challenges in the rectifier can be avoided; the current distortion at zero-crossing points is removed and IR limitation is inherently satisfied with no need for offset voltage injection.

<table>
<thead>
<tr>
<th>region</th>
<th>$V_p$</th>
<th>$V_n$</th>
<th>Control signal selector</th>
<th>Gate signal distributor</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>$V_{oa}$</td>
<td>$V_{ob}$</td>
<td>$E - (2V_{c} + V_{b})$</td>
<td>$S_a, S_b, S_c$</td>
</tr>
<tr>
<td>II</td>
<td>$V_{oa}$</td>
<td>$V_{oc}$</td>
<td>$E - (2V_{a} + V_{c})$</td>
<td>$S_a, S_b, S_c$</td>
</tr>
<tr>
<td>III</td>
<td>$V_{oa}$</td>
<td>$V_{oc}$</td>
<td>$E - (2V_{a} + V_{c})$</td>
<td>$S_a, S_b, S_c$</td>
</tr>
<tr>
<td>IV</td>
<td>$V_{oa}$</td>
<td>$V_{ob}$</td>
<td>$E - (2V_{b} + V_{c})$</td>
<td>$S_a, S_b, S_c$</td>
</tr>
<tr>
<td>V</td>
<td>$V_{oa}$</td>
<td>$V_{oc}$</td>
<td>$E - (2V_{b} + V_{a})$</td>
<td>$S_a, S_b, S_c$</td>
</tr>
<tr>
<td>VI</td>
<td>$V_{oa}$</td>
<td>$V_{oc}$</td>
<td>$E - (2V_{c} + V_{a})$</td>
<td>$S_a, S_b, S_c$</td>
</tr>
</tbody>
</table>

The whole closed loop control structure is presented in Fig. 6, which consists of two control loops: the inner current loop providing sinusoidal input current and the outer voltage loop applied to achieve fixed voltage at the rectifier output. It is worth mentioning that contrary to the proposed method, in the existing switching strategies, utilizing an auxiliary feedback loop is inevitable to overcome the dc link voltage unbalance.

![Fig. 6 — Closed-loop control system.](image)

In Fig. 6, the reference current amplitude is derived based on the error between the dc voltage reference ($V_{abc}^*$) and its measured value ($V_{abc}$). The angle of the three-phase grid voltage is derived through the PLL block, which is used to generate the current reference ($I_{abc}^*$) in phase with $V_{abc}$. Input current error is then passed through a PI controller, providing the reference signals ($V_{abc}^*$) for the proposed CLD-DPWM method.

3. NEUTRAL POINT ANALYSIS

Referring to decoupled circuit for Vienna rectifier in Fig. 3 and above analysis, it can be found that positive boost rectifier will transfer its energy to $C_1$, while the negative boost rectifier will transfer its energy to $C_2$. As a result, equal power is transferred to $C_1$ and $C_2$ during a fundamental cycle and though, dc link capacitors will be naturally balanced.

The following mathematical analysis is carried out as a proof to the fact. Assuming the three phase input voltages and currents to be sinusoidal and balanced, yields

$$V_a = \alpha \sin \omega t, \quad I_a = I_m \sin(\varphi - \theta) \quad (6)$$

$$V_b = \alpha \sin(\omega t - 120^\circ), \quad I_b = I_m \sin(\varphi - 120^\circ) \quad (7)$$

$$V_c = \alpha \sin(\omega t + 120^\circ), \quad I_c = I_m \sin(\varphi + 120^\circ) \quad (8)$$

where $I_a = d_ia + d_bib + d_cic$.

The mean value of the neutral point current during a modulation period can be obtained as follows

$$i_n = \frac{1}{T} \int_{0}^{T} i_n dt \quad (9)$$

and is expressed through (9)–(13)

$$i_{na} = d_p \times i_a + d_b \times i_b + d_c \times i_c$$

$$i_{nb} = d_p \times i_b + d_a \times i_a + d_b \times i_c$$

$$i_{nc} = d_p \times i_c + d_a \times i_a + d_b \times i_b$$

The above equation can be generalized for regions (II–VI) and is expressed through (9)–(13)
\[ i_{nY} = i_Y + i_b + i_d \times \delta \]

\[ = [1 - (2\pi v - V_d)] \times i_Y + [1 - (2\pi v - 2V_d)] \times i_b \times \delta \]

(13)

Summation of (9)–(13), leads to the zero current injection to dc link neutral point during a fundamental cycle

\[ i_n = i_{nH} + i_{nIII} + i_{nIV} + i_{nY} + i_{nY} = 0 \]

(14)

Accordingly, it can be concluded that in the proposed scheme for Vienna rectifier, the neutral point voltage will not deviate from its equilibrium point and in consequence, the dc link capacitors are naturally balanced with no requirement for an additional feedback loop.

4. SWITCHING LOSS CALCULATION

Switching loss is the power dissipated during turning on and turning off the switching devices and is directly proportional to the switching frequency. This loss is calculated for the switch and anti-parallel diode. Switching loss in an inductive system is introduced as below [30]

\[ P_{sw,T} = (E_{on} + E_{off}) \times f_{sw} \]

\[ \Rightarrow P_{sw,T} = f_{sw} V_{DS} t_{sw(on)} \left( E_{on} + t_{sw(off)} \right) \pi \]

(15)

\[ P_{sw,D} = (E_{on} + E_{off}) \times f_{sw} \approx E_{off} \times f_{sw} \]

\[ \Rightarrow P_{sw,D} = \frac{1}{2} Q_{\alpha} V_{D} f_{sw} \]

(16)

where \( P_{sw,T}, P_{sw,D} \) are switching loss of the switch and diode respectively, \( f_{sw} \) is the switching frequency, \( V_{DS} \) is the off-state voltage across the switch and \( I_{off} \) is the maximum switching current. Likewise, \( I_{on} \) and \( E_{off} \) are the switch on-state and off-state energy respectively. \( Q_{\alpha} \) is the diode reverse recovery charge, \( I_{on(on)} \) and \( E_{off(on)} \) are the switching turn on and turning off times respectively and \( V_D \) is thepeak voltage across diode.

In this paper, following parameters are considered to calculate the switching loss of the proposed configuration:

\[ t_{sw(on)} = 75 \text{ms}, \quad t_{sw(off)} = 84 \text{ms}, \quad Q_{\alpha} = 400 \text{nC}, \quad r_d = 0.1 \Omega, \quad R_{bd(on)} = 0.46 \Omega, \quad f_{sw} = 10 \text{kHz} \]

It should be noted that, in the presented discontinuous switching strategy each switch is pulse width modulated during just 240° of line cycle. Hence, compared with the continuous strategies, the number of turning-on and turning-off times of each switch and its corresponding current diode in bridge structure, will decrease by a factor of 1/3, according to eq. (17) and (18):

\[ N_{on} = N_{off} = \frac{f_{sw}}{3} \] \[ \Rightarrow N_{on} = N_{off} = \frac{2}{3} \times \frac{f_{sw}}{f_1} \]

(17)

\[ P_{sw} = f_1 \left( \frac{2}{3} \times \frac{f_{sw}}{f_1} E_{on} + \frac{2}{3} \times \frac{f_{sw}}{f_1} E_{off} \right) = \frac{2}{3} f_{sw} \left( E_{on} + E_{off} \right) \]

(18)

where \( N_{on} \) and \( N_{off} \) are the number of turning-on and turning-off times of each switch and \( f_1 \) is the fundamental frequency.

4. INPUT INDUCTOR DESIGN

For the purpose of input inductor design, it is assumed that \( d_i > d_e \) and the positive boost converter, Fig. 4(a), is considered. Hence, the inductor is charged for the period of \( d_i T_{sw} \) and discharged for the period of \((1 - d_i) T_{sw}\). The current waveform of \( L \) during a switching cycle is depicted in Fig. 7.

Considering the equivalent circuit in Fig. 3 (for region 1), the inductor current is defined as eq. (19) during off cycle \((1 - d_i) T_{sw}\): \[ i(t) = i_0 - \frac{v_{in}}{L} \left( i_{sw} \right) dt = i_0 - \frac{\left( V(t) - E \right) \left( 1 - d_i \right) T_{sw}}{L}. \]

(19)

Hence,

\[ \Delta i_{on} = \frac{\left( V(t) - E \right) \left( 1 - d_i \right) T_{sw}}{L}, \]

where \( i_0 \) is the initial inductor current and \( \Delta i_{on} \) is the maximum inductor current ripple.

By inspecting the waveforms in Fig. 2, the positive and negative converter voltages \( V(t), V_D(t) \) are extracted as:

\[ V_p(t) = V_e \cos (\omega t - 60^\circ), \quad 0 < \omega t < 60^\circ \]

\[ V_n(t) = -V_e \cos (\omega t), \quad -60 < \omega t < 60^\circ. \]

Substituting (21) in (5) obtains:

\[ \left( 1 - d_i \right) = \frac{2v_e \cos (\omega t - 60)^\circ \Delta T_e - v_e \cos (\omega t)}{E}. \]

(22)

Correspondingly, substituting eq. (22) in (20) and solving the following differential equation for \( \omega t \), yields:

\[ \frac{d}{dt} \left( \Delta i_{on} \right) = 0 \Rightarrow \omega t = 30^\circ. \]

(23)

The above equation implies that the maximum current ripple occurs at \( \omega t = 30^\circ \) and the positive and negative voltages are derived:

\[ V_p = V_e = 0.866V_e \quad , \]

\[ V_n = V_b = -0.866V_e. \]

(24)

Substituting eq. (22) and (24) in (20), the maximum inductor current ripple can be achieved:

\[ \Delta i_{on} = -\frac{0.866V_e \times \left( 0.866V_e - E \right) T_{sw}}{E}. \]

(25)

Rearranging eq. (25), the proper inductor value for a specific current ripple will be extracted:

\[ L = \frac{0.866V_e \times \left( 0.866V_e - E \right) T_{sw}}{\Delta i_{on}}. \]

(26)

5. SIMULATION AND EXPERIMENTAL VERIFICATION

To verify the performance of the proposed CLD-DPWM
technique, a 1 kW Vienna rectifier is simulated in MATLAB/SIMULINK. The simulation parameters are listed in Table 3. The acceptable range for modulation index in Vienna rectifier is achieved as [31]:

\[ M_a \leq \frac{2}{\sqrt{3}} \Rightarrow \sqrt{3} V_m \leq V_{dc} \]  

(27)

where, \( V_m \) and \( V_{dc} \) are mains voltage amplitude and dc link voltage, respectively.

Furthermore, it is worth mentioning that the proposed control algorithm imposes more boosting voltage than other modulation strategies. For instance, considering region I in Fig. 2, the following condition should be met:

\[ V_{ac} > \frac{V_m}{2} \]  

(28)

which occurs at \( \omega t = 30^\circ \) and the minimum voltage over positive boost converter (Fig. 4 (a)) is obtained as:

\[ \frac{V_{ac}}{2} = V_m \sin(\omega t + 120) - V_m \sin(\omega t) = \frac{3}{2} V_m. \]  

(29)

Thus, the minimum output dc voltage will be:

\[ V_{DC_{min}} = 3 V_m = \sqrt{3} V_{LL_{max}}. \]  

(30)

where \( V_{LL_{max}} \) is the peak line voltage.

As in eq. (30), \( V_{DC_{min}} \) is 73 % more than the line voltage obtained through other modulation strategies for Vienna rectifier, which makes the structure compliant with high voltage industrial installations.

Table 3  
Simulation parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input line voltage</td>
<td>( V_{LL} = 122 ) V</td>
</tr>
<tr>
<td>Input inductor</td>
<td>( L = 3 ) mH</td>
</tr>
<tr>
<td>De link capacitor ( C_1, C_2 )</td>
<td>1300 ( \mu F )</td>
</tr>
<tr>
<td>De link reference voltage</td>
<td>( V_{ref} = 300 ) V</td>
</tr>
<tr>
<td>Switching frequency ( f_s )</td>
<td>10 kHz</td>
</tr>
<tr>
<td>Line frequency ( f_m )</td>
<td>50 kHz</td>
</tr>
</tbody>
</table>

Rectifier 3-phase input current and its harmonic spectrum are illustrated in Figs. 8 and 9, respectively. It can be observed from Fig. 8, that the current distortions at zero-crossing points are essentially removed, since the phase with near-zero current is clamped to the neutral point by keeping its switch on.

As in [19], the rectifier input current in the proposed method, like other existing discontinuous approaches, is subjected to distortion and its THD is slightly increased in comparison to the continuous strategies.

According to Fig. 9, the input current harmonic distortion in the proposed method is 2.87 % versus 1.88 % for continuous approaches. However, it satisfies IEEE 519 (i.e. max. of THD for each order: 5 %). Consequently, taking into account the aforementioned advantages of the proposed method, this minor increase in THD can be justified. It should be noted that in the above charts, the fundamental components exceed the limits and this is due to the better illustration of other harmonic contents.

Fig. 8 – Three phase grid current.

![Fig. 8 – Three phase grid current.](image)

Fig. 9 – FFT analysis of input phase current a) existing CB-PWM method, b) proposed DPWM method.

![Fig. 9 – FFT analysis of input phase current a) existing CB-PWM method, b) proposed DPWM method.](image)

The corresponding waveforms of single phase input voltage/current and dc output voltage are shown in Fig. 10. In the presence of the proposed discontinuous switching strategy, the unity power factor is achieved, and IR is satisfied with no need for an extra offset voltage injection. Moreover, the dc bus voltage accurately tracks the reference and the voltage ripple will be kept within less than 1 %.

Fig. 10 – Simulation results for: a) input current and voltage, b) dc link voltage.

![Fig. 10 – Simulation results for: a) input current and voltage, b) dc link voltage.](image)

To prove the effectiveness of the proposed strategy in terms of switching loss reduction, the corresponding switching signal in phase (a) is presented in Fig. 11.

Fig. 11 – Phase (a) switching signal.

![Fig. 11 – Phase (a) switching signal.](image)
mentioned previously, in the existing CB-DPWM method [19], the non-switching range is varied between minimum and maximum values to meet IR, depending on $M_d$.

A comparison between the conventional CB-CPWM and the proposed CLD-DPWM methods in terms of switching loss and current THD has been carried out and the results are summarized in Table 4.

<table>
<thead>
<tr>
<th></th>
<th>Existing CB-CPWM</th>
<th>Proposed CLD-DPWM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching loss of MOSFETs and diodes (W)</td>
<td>5.14</td>
<td>3.42</td>
</tr>
<tr>
<td>Input current THD (%)</td>
<td>1.88</td>
<td>2.87</td>
</tr>
</tbody>
</table>

Phase (a) voltage on both the grid side and the switch side are shown in Fig. 12. As in the figure, the switch side voltage is clamped to ($-V_{dc}/2$), 0, ($+V_{dc}/2$). Furthermore, since the phase with transitional state is clamped to zero during each 60˚ region, two zero intervals occur in the switch side voltage waveform.

The performance of the proposed method is further validated through representation of dc link voltages $V_{C1}$ and $V_{C2}$ as well as the voltage ripple in the sub-window in Fig. 13. As in the figure, the capacitor voltages are essentially well balanced, and no extra feedback loop or offset voltage injection is required.

Figure 14 shows the dynamic balancing process in which the initial voltages on dc link capacitors are unbalanced as $V_{C1} = 200$ V and $V_{C2} = 100$ V and they converge after a very short time interval.

The instantaneous variations as well as the average value of neutral point current are illustrated in Fig. 15. As in the figure, the neutral point current variation in each switching cycle is completely symmetrical and hence, the average current injected into the neutral point has the zero value.

Moreover, the input voltage is subjected to two step from 70 V to 40 V at 0.3 s (which is the boundary of the input voltage range for $V_o = 300$ V) and from 40 V to 70 V at 0.6 s. As illustrated in Fig. 16, the converter is well stable at its reference value of 300 V, despite the step change in the input voltage.

To further verify the effectiveness of the proposed control strategy, an experimental prototype is built at laboratory scale. The experimental laboratory prototype is depicted in Fig. 17. The power stage consists of dual common cathode ultrafast rectifiers (FEP30J) and Si MOSFETs (IRFP260N), and the control system is executed in MCU TMS320F28335 DSP with the switching and sampling frequency of 10 kHz. The input voltage is 40 Vrms / 50 Hz and the input inductors are 5 mH. The two dc-link capacitors connected in series at the dc-side are 1300 µF, and the load resistance is 143 Ω. Moreover, the dc reference voltage is 190 V.
Figure 18 presents grid voltage and input current in phase \((a)\). The figure verifies the simulation results in terms of power factor and current distortion at the vicinity of zero-crossing points. Figure 19 illustrates the experimental results of phase \((a)\) current, line to line voltages at the grid side \((V_{ab})\) and the switch side \((V_{AB})\).

The five-level characteristic of \(V_{AB}\) is apparent from the waveform. Figure 20 shows the experimental results of dc-link voltages: \(V_{c1}, V_{c2}\) and \(V_{dc}\). The waveforms well prove the self-balancing behavior of the proposed method, with no requirement for an extra sensor in the experimental setup.

In order to show the dynamic performance of the system, the experimental setup is tested under a load step change and the corresponding experimental results are presented. Figure 21 shows the operation of the proposed converter with the 40\% load step up and the terminal voltage of \(V_{dc}=190\,\text{V}\). The load resistance changes from \(R=243\,\Omega\) to \(R=143\,\Omega\). As can be seen in the figure, the converter is well regulated at this step load change and output voltage returns to steady-state mode within less than 0.08 s.

### 6. CONCLUSIONS

This paper introduced a discontinuous modulation strategy based on circuit-level decoupling concept for Vienna rectifier. According to the proposed strategy, the rectifier structure is decoupled into two two-level boost converters in every 60\° region. In comparison to the other existing strategies for Vienna rectifier, this method has the merit of simple digital implementation and lower switching loss. Advantages of the proposed DPWM scheme are highlighted by simulation results and can be summarized as:

1. Control design simplification: the control core can be implemented by all existing dc-dc converters control methods and only one carrier wave is needed.
2. Switching loss reduction by one-third: just two of three switches in the configuration are modulated under high frequency and the other one is kept on during the whole region.
3. Inherent neutral point balancing: no need for offset voltage injection or an additional feedback/feedforward loop to balance dc bus capacitor voltages.
4. No current distortion near zero crossing point.
5. Compliant with IR without offset voltage injection.

The detailed analysis of the simulation results and experimental tests on a 250 W and 10 kHz laboratory prototype well proves the effectiveness of the proposed modulation strategy.

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