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THE PARALLEL CONNECTION OF PHASE-SHIFTED FULL-BRIDGE DC-DC CONVERTERS

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Key words: Automotive dc-dc converter design, Current sharing, Phase-shifted full-bridge, Peak current mode control.

When designing a high-power dc-dc converter for an Electrical Vehicle (EV) the main objectives are high efficiency, high reliability and low costs. Achieving high efficiency for wide load and high reliability for a dc-dc converter by using a single power module may be extremely difficult if the efficiency at light load must be very high and redundancy is required. Very often, the solution is to divide the total power over several power modules operating in parallel. When the dc-dc converters are operated in parallel, the load sharing can be a severe issue if no active current sharing is implemented. In this paper, several current sharing techniques are investigated and a new current sharing method for parallel connection of Phase-Shifted Full-Bridge (PSFB) converters is proposed. The new control solution is also implemented on a prototype to validate the simulations with experimental results.

1. INTRODUCTION

Parallel connection of several dc-dc converters is very often preferred instead of a single converter with equivalent power due to following benefits:

- uniform losses distribution and increased cooling surface;
- reduction of input and output capacitors ripple by using interleaved operation;
- high efficiency at light load by shutting down of one or several parallel modules;
- high reliability and redundancy by disconnecting failed modules;
- smaller power semiconductors and smaller magnet components.

The parallel connection of dc-dc converters requires a current sharing mechanism to guarantee equal current distribution and to avoid electrical and thermal stress among modules. If no current-sharing mechanism is implemented, even small constructive differences between modules can lead to severe output current unbalance [1].

There are two main approaches for load sharing. The first one, known as "droop" method [2], is based on the high output impedance of each power module. Although, this is simple to implement as it does not require any exchange of information between converters and it have a poor output voltage regulation. For this reason, this approach is not used for high performance applications. The second approach, known as active current-sharing [3-5], is used to overcome the main drawbacks of the droop method.

Active current-sharing control can be divided in two categories: current mode and voltage mode control. The current mode control uses the peak or average current as reference for the modules in parallel. In the voltage mode control, the voltage loop reference is modified to get even output currents for modules running in parallel.

In this paper, the main parallel connection techniques of dc-dc converters are reviewed and a new current sharing method for the parallel connection of PSFB converters is proposed.

The work is organized as follows. Section 2 briefly shows different methods of parallel connection of dc-dc converters: "droop" technique, common point voltage feedback control, average current mode control and peak current mode control (PCMC). The PCMC method proved to be the best approach. Thus, in Section 3, two operating modes for PCMC are investigated: synchronous and interleaved. Both operation modes are analyzed by numerical simulations. Due to limitations of the microcontroller used in the physical prototype, only synchronous operation mode is verified experimentally in Section 4. Finally, the conclusions are summarized.

2. METHODS FOR CONNECTING DC-DC CONVERTERS IN PARALLEL

2.1. "DROOP" METHOD

The method assumes that the dc-dc converters are designed with a finite output resistance. Therefore, the output voltage will drop proportional with the output current. If the output resistance of each converter connected in parallel is properly adjusted for a particular operating point, the converters will share the output current in all load conditions. The block diagram of the droop method is shown in Fig. 1.

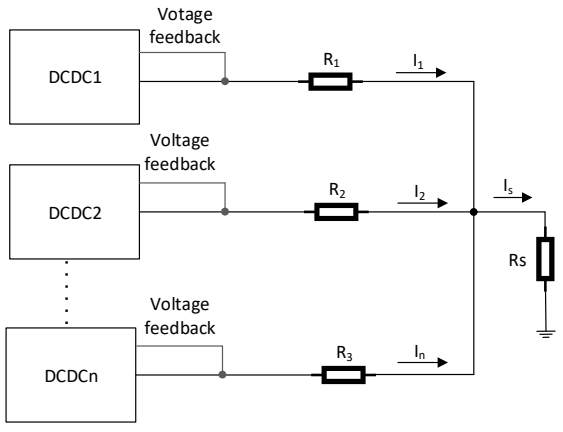

Fig. 1 – "Droop" method for dc-dc converters connected in parallel.

While this method is widely used as is simple to implement, it presents some important disadvantages:

- the dc-dc converters must be initially adjusted to get even current distribution among modules;
- it is prone to current unbalance with time, due to components parameter drift generated by electrical stress or aging;
- poor accuracy of the output voltage.

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2.2 COMMON POINT VOLTAGE FEEDBACK CONTROL

This method uses a single voltage control loop and the feedback is taken from a common point for all converters connected in parallel. The duty-cycle is the same for all modules and if the modules are identically designed, acceptable current sharing is obtained. The block diagram is presented in Fig. 2.

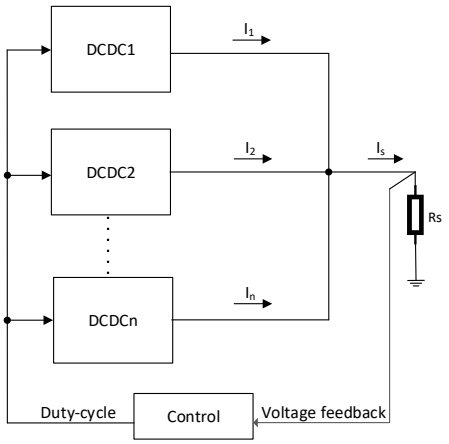


Fig. 2 – Common point voltage feedback control.

As the duty-cycle is the same for all modules connected in parallel, the output currents are equal only if the converters are identical.

In practice, due to components tolerances and physical constraints, is impossible to build two identical converters, so current unbalance between modules will inherently appear.

The most important disadvantage of this method is the sensitivity to small duty-cycle differences between modules generated by the drivers, switches activation voltage or components tolerances.

Very small duty-cycle differences can lead to severe output current unbalance between modules. This may cause electrical and thermal stress on modules which are delivering most of the current leading to premature aging or even failure.

2.3 AVERAGE CURRENT MODE CONTROL

This method consists in regulating the output current of each module by using the average current information. The average current is measured at the output of each module and shared over a dedicated current sharing bus. In this way, the duty-cycle of each converter is adjusted to obtain equal output currents among parallel modules.

In order to implement this solution, a current sensor is needed for each converter output and each converter to have its own voltage regulator. The block diagram of the average mode control is shown in Fig. 3.

This method offers a good load sharing accuracy between parallel modules if the output load is constant or varies slowly. It provides also redundancy in case of one module fails. During startup or load transients, the average current regulation is usually not fast enough to equalize the output currents of the modules and dynamic unbalance may appear. This effect must be carefully evaluated to prevent that some modules are not exposed to electrical or thermal overstress which may lead to premature aging or even failure.

In applications with large load steps and fast transients the average current regulation for current balancing may not be the best solution.

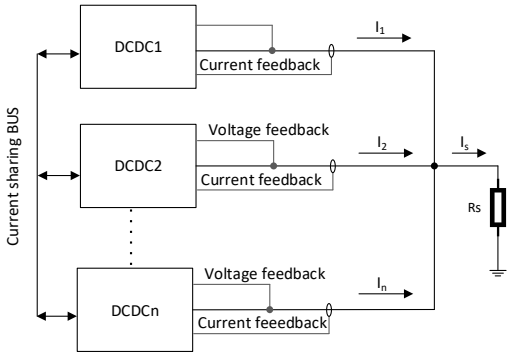


Fig. 3 – Average current mode control.

The main advantages of this method are:

- good load sharing accuracy (with constant load);
- redundancy in case of one module fails;
- good accuracy of the output voltage

The main disadvantages are:

- current unbalance during startup and load transients;
- complexity (dedicated integrated circuit is usually required);
- current sensors at the output of each converter is needed.

2.4 PEAK CURRENT MODE CONTROL (PCMC)

The Peak Current Mode Control method consists in regulating the peak current of the dc-dc output inductor. To implement this current sharing mechanism, each converter must have its own current regulator. The peak current reference is imposed by the voltage regulator and is common for all modules connected in parallel. In the Fig. 4, the block diagram of the PCMC current sharing mechanism is presented.

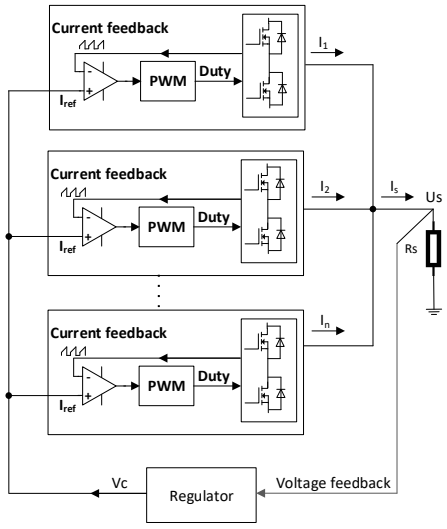


Fig. 4 – Peak Current Mode Control.

As the current reference is the same for all converters, they will all have the same peak inductor current. This ensures even current distribution between parallel modules at constant load but also during dynamic transitions.

Measuring the output inductor current with good accuracy is usually difficult as it operates at high currents and it has large voltage swings across terminals. A simpler and more efficient way is to measure the dc-dc converter input current by using of a current transformer. A current transformer is normally included anyhow in the primary side of the converter for overload or short circuit protection.

The main advantages of the PCMC are:

- precise current sharing during steady and dynamic load;
- fast transient response;
- inherent overcurrent protection;
- no need for DC decoupling capacitor for power transformer;
- no need for additional current sensor at the dc-dc output (exiting input current transformer can be used).

3. NUMERICAL SIMULATIONS FOR THE PROPOSED PCMC METHOD

The operation of a single PSFB dc-dc converter (Fig. 5) was presented by the authors in reference [6-7].

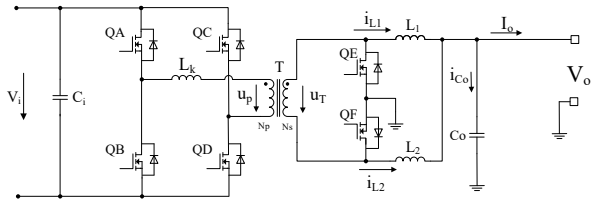


Fig. 5 – PSFB dc-dc converter.

This topology is commonly used for energy conversion from high voltage battery to the 12V battery and for supplying the low voltage network in hybrid and electric vehicles. The main benefits of the topology are:

- high power density;
- high efficiency due to soft switching;
- galvanic isolation.The design parameters for the PSFB dc-dc converter are presented in Table 1.

Table 1

Main converter design parameters.

Input voltage	200V - 420V
Output voltage	14V
Output current	230A (2x115A)
Output power	3.2kW (2x1.6kW)
Switching freq.	200kHz

3.1 SINGLE MODULE SIMULATION

The topology described in Fig. 5 is numerical simulated using PCMC method. Thus, the power schematic of the converter is shown in Fig. 6.

The control of the converter consists in four main blocks: the voltage regulator, the ramp generator, the PWM module and the clock generator. The voltage regulator provides the peak current reference for the positive input of the PWM module.

As the PCMC presents a risk of subharmonic oscillations at duty-cycles higher than 50%, slope compensation [8] is required and is implemented by using a ramp generator, which creates an artificial ramp that is summed with the sensed primary current. The resulted signal is then used as negative input for PWM module. The clock module provides the clock signal for the PWM module.

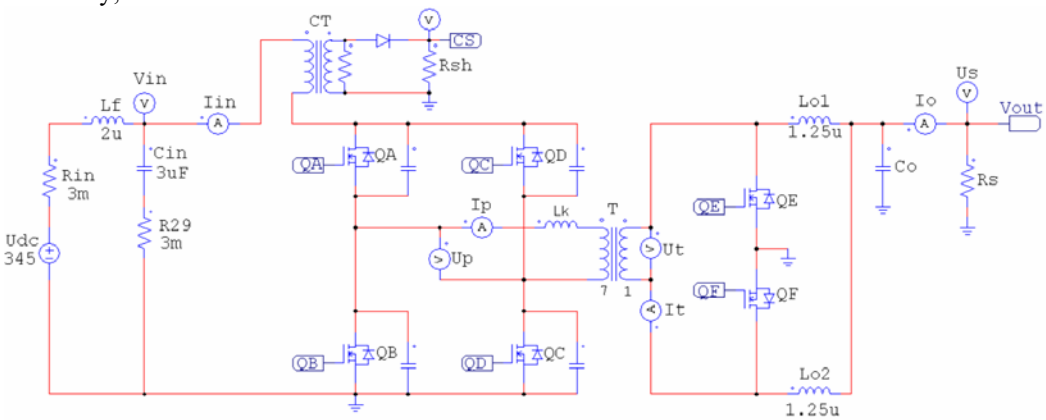


Fig. 6 – The power schematic of the PSFB dc-dc converter.

The proposed control schematic diagram is presented in Fig. 7 and the simulation results of a single converter are presented in Fig. 8.

The converter operates at nominal output power with 350V input voltage, 14V output voltage and 115A output current. The primary voltage Up of the power transformer is formed due the phase shift between full bridge legs QA, QB respectively QC, QD.

The converter phase shift (duty-cycle) is controlled by the current reference "Ipeak_ref" imposed by the voltage regulator. The peak primary current is sensed by current transformer. When its value equals the current reference, the conduction interval is stopped by the comparator.

In this way, both positive and negative peaks of the primary current are equal canceling any dc component which usually appears in voltage mode control converters. This creates two important advantages of PCMC.

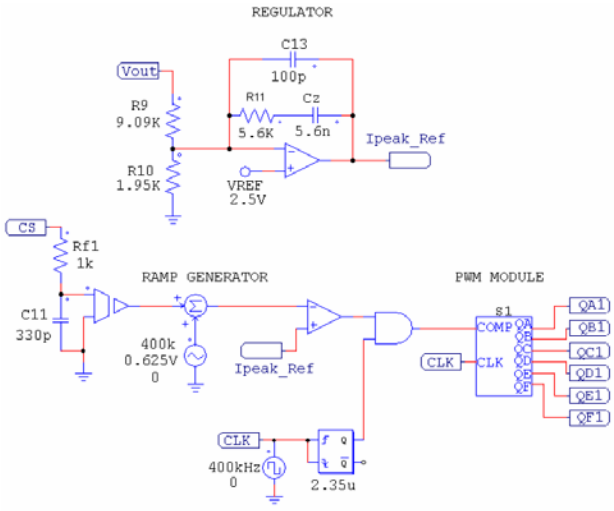


Fig. 7 – Proposed control schematic of single PSFB dc-dc converter.

First, the power transformer decoupling capacitor can be removed. Second, if the same current reference is imposed on other dc-dc modules, they will all have the same peak input currents and will share also the output currents.

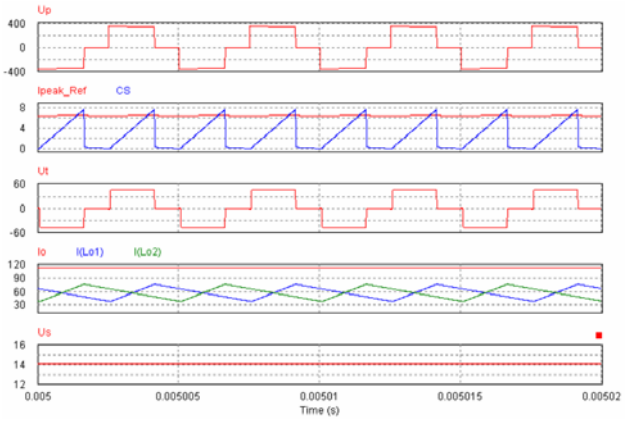


Fig. 8 – Simulation results of single PSFB dc-dc converter.

3.2 TWO PARALLEL MODULE SIMULATION

The schematic of two PSFB dc-dc converters connected in parallel is presented in Fig. 9. In order to reduce the complexity of the analysis, the converters are considered to be identical from design point of view.

The proposed control schematic for PCMC is presented in Fig. 10. It contains a voltage regulator which provides the current reference for all modules, artificial ramp generator, PWM module for each converter and individual input current sense.

The connection in parallel of the dc-dc converters, that use PCMC method, can be implemented in two ways. One way is to use synchronized PWM clocks for all modules (synchronous operation). Second way is to use phase-shifted clocks (interleaved operation).

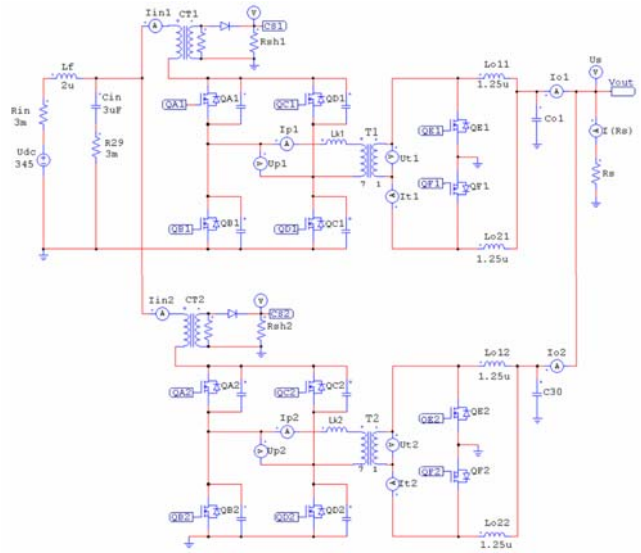


Fig. 9 – Power schematic of two PSFB converters connected in parallel.

For interleaved operation, the PWM clocks are running with a phase shift equal with 360° divided by the number of modules connected in parallel. Both operation modes are analyzed by simulations. Due to limitations of the microcontroller used in the physical prototype, only synchronous operation mode is verified experimentally.

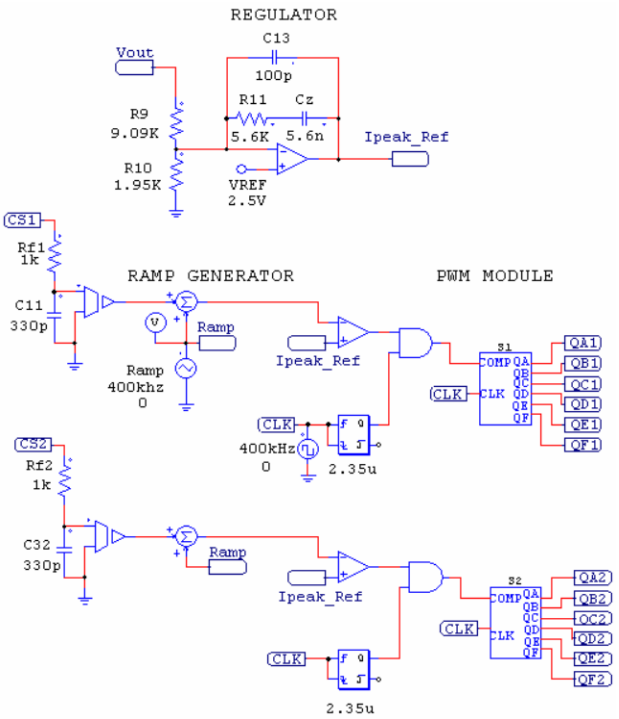
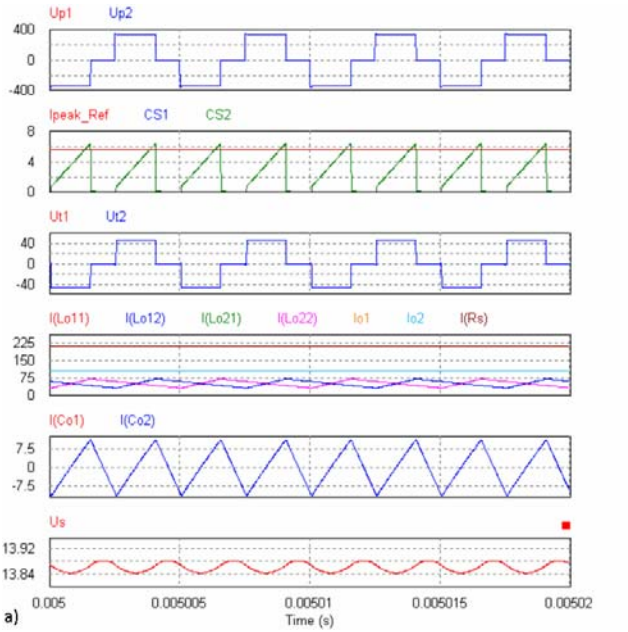


Fig. 10 – Proposed control schematic for parallel operation.

The simulation results for parallel operation using PCMC method are provided in Fig. 11. The waveforms notations correspond to Fig. 9.

For comparison, both operation modes, synchronous and interleaved are presented. In the case of synchronous operation, due to the using of same clock, the waveforms of the two converters overlap, so only one waveform is visible. As can be observed, when using interleaved operation, the output capacitor ripple current and output voltage ripple are significantly reduced [9].

The interleaved operation may allow a reduction of the output capacitance value compared with synchronous mode. In regards of current sharing, both operation modes ensure precise current sharing between parallel connected converters.



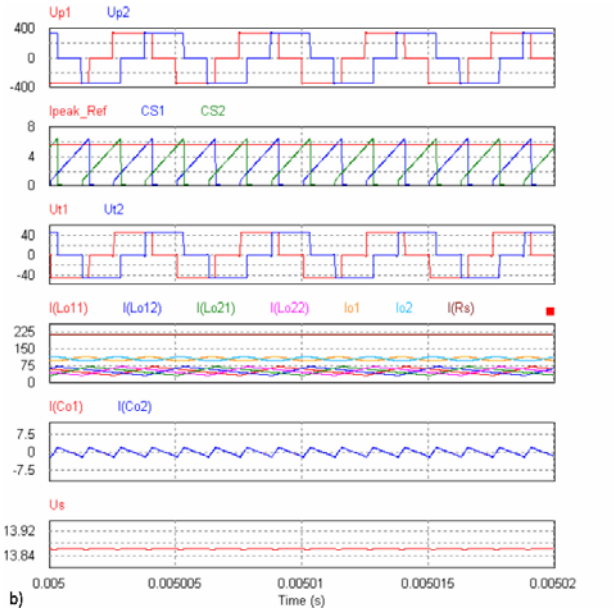


Fig. 11 – Simulation results for parallel operation.
a) Synchronous mode, b) Interleaved mode.

In order to chek the dynamic performance of PCMC solution, a load step is applied during parallel operation. The current step is from 100 A to 200 A (50 % to 100 % of nominal output current). For comparison, both operation modes are presented: syncronous technique in Fig. 12 and interleaved mode in Fig. 13.

The simulation results prove that the PCMC method ensures precise current sharing between parallel modules even during severe load dynamics. This control also provides a fast transient response, which is a must for high-performance dc-dc converters. It has been observed that is no visible difference in terms of dynamic behavior between synchronous and interleaved operation modes.

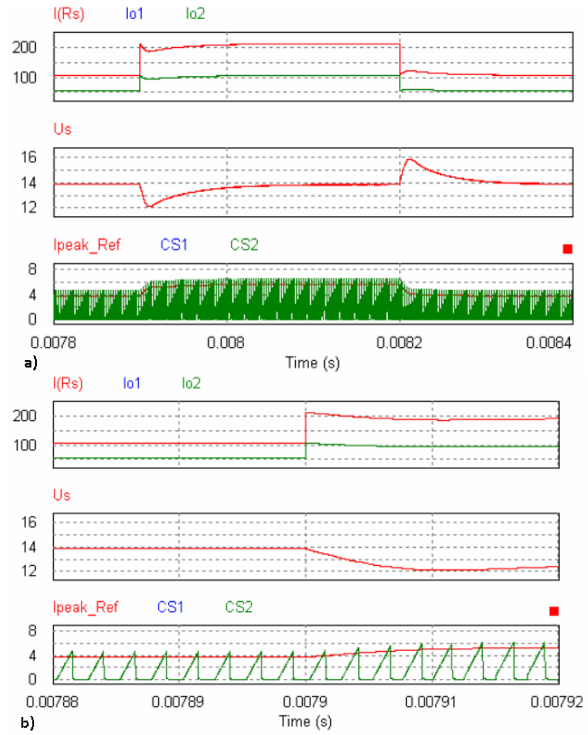


Fig. 12 – Load step response of the PSFB using synchronous PCMC.
a) Full dynamic response, b) Rising edge current sharing.

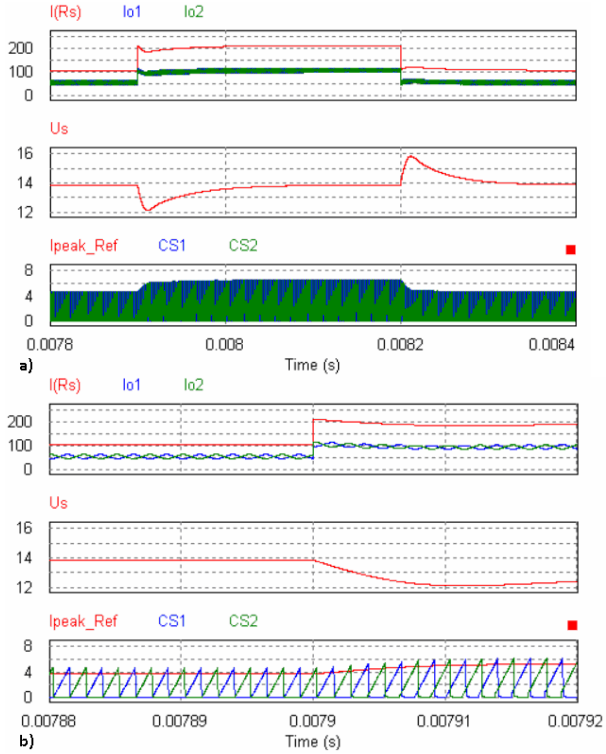


Fig. 13 – Load step response of the PSFB using interleaved PCMC.
a) Full dynamic response, b) Rising edge current sharing.

4. EXPERIMENTAL RESULTS

In order to validate the simulation results, the proposed synchronous PCMC method was implemented on a dc-dc 400 V/14 V isolated converter with 3.2 kW nominal power.

The converter consists in two identical PSFB modules connected in parallel. Each module has a nominal power of 1.6 kW. The control of both modules is implemented using a single TMS320F28069 DSP (Digital Signal Processing) microcontroller.

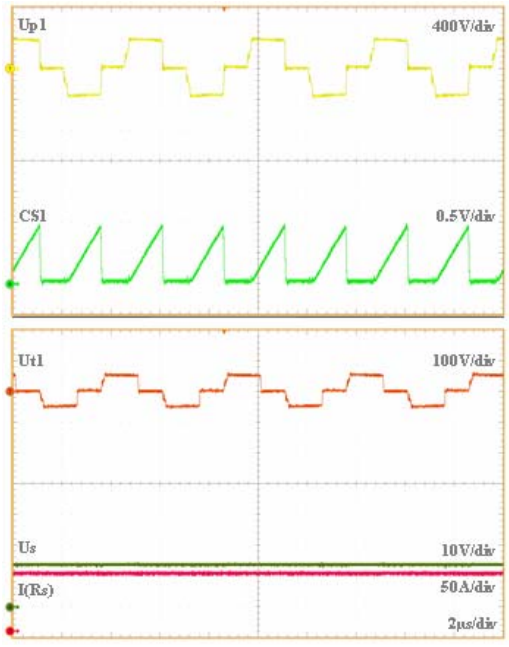


Fig. 14 – Experimental results
for single module operation using the proposed PCMC method.

In Figs. 14 and 15 the experimental results for two operating modes are presented: single and two modules operating in parallel. The waveforms notations correspond to the ones from Fig. 9.

In the first case, the module two is turned off to save power. This operation mode is used to increase the converter efficiency when the output load is lower than nominal current of one module.

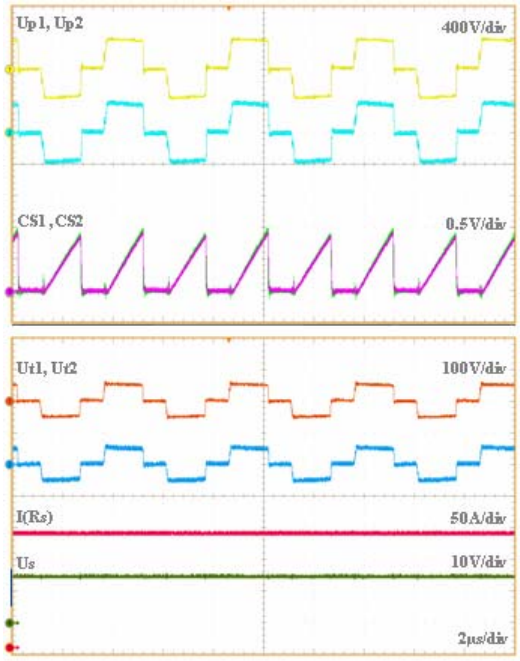


Fig. 15 – Experimental results for two modules operating in parallel using the proposed PCMC method.

5. CONCLUSIONS

In this paper, the most known current sharing methods for dc-dc converters have been evaluated. The scope was to find the optimum solution for connecting in parallel of PSFB dc-dc converters. The proposed PCMC method proved to be the best approach, offering excellent input and output current sharing together with fast transient response. In addition for this control technique, two operating modes have been investigated: synchronous and interleaved.

The synchronous PCMC solution is easier to implement as only one PWM clock is used for all modules. The main drawback of this solution is the input and output capacitor current ripple which can be very large. In order to reduce the capacitors current ripple, an interleaved PCMC technique has been investigated.

The interleaved PCMC mode offers the same current sharing and transient performance as the synchronous PCMC mode but with significant input and output current ripple reduction. The ripple reduction is maximum when the converter duty-cycle reaches 50%. At this point the input and output currents ripple are in opposite phase offering full ripple cancellation. Another benefit of the proposed PCMC strategy, which is very important for full-bridge converters, is the dc voltage cancellation in the primary of power transformer. This allows removing of the dc decoupling capacitor which is mandatory for voltage mode full bridge converters. This helps to improve the efficiency and to reduce the costs of the converter.

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