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LOW-VOLTAGE ALL-NMOS FOUR-QUADRANT CURRENT MULTIPLIER

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Key words: Analog multiplier, Current-mode circuits, Squarer, MOS analog circuits, Low-voltage circuits.

This paper presents a low-voltage four-quadrant current-mode multiplier circuit using all-NMOS technique. The circuit is constructed using current-squaring function circuits and simple current mirrors, where all small-signal currents pass through only NMOS transistors. The proposed current multiplier is simple and suitable for low-voltage, low-power operation. The circuit performances were demonstrated by PSPICE simulations with TSMC 0.35-μm CMOS process. To show the basic function of the proposed circuit, the frequency doubling and amplitude modulating circuits have been performed and simulated.

1. INTRODUCTION

Analog multiplier is one of the essential circuits that can readily be found in the design of many signal conditioning and processing applications [1, 2]. It is not only used as an analog computation circuit, but also as a programming circuit element in communication systems such as, peak detectors, modulators, synthesizers and artificial neural networks and fuzzy logic controllers [3]. Several attempts to design current-mode multiplier circuits in CMOS technology are already available in the literature [4–11]. However, the interesting multipliers presented in [4–[6] require that the transconductance parameters of PMOS and NMOS transistors are needed to be identical, *i.e.* $K_p = K_n$. This approach seems to be very difficult from a practical viewpoint, because the K_p and K_n values of MOS transistors strongly depend on the fabrication process. In [7–8], the translinear loops of MOS transistors operating in the weak inversion mode are used as the fundamental building blocks in the circuit realizations. This method has the advantage of low-power consumption, but the dynamic range of the circuit is very small, in order of < 2 μA. Therefore, the usefulness of the circuit is rather limited. A four-quadrant current-mode multiplier based on a new current squaring function circuit has been proposed in [9]. However, the circuit needs one or more additional circuit components to provide triple input current signals (i_x, i_y and $i_x + i_y$) and minus input current signals ($-i_x$, $-i_y$ and $-(i_x + i_y)$), where i_x and i_y are the inputs to be multiplied. Also, it employs the dual-polarity supply voltages of ±1.5 V. In [10], a low-voltage four-quadrant CMOS current multiplier circuit has also been reported. The circuit is based on the use of four compact voltage-to-current converter cells, able to operate at low voltage level of 1.5 V. However, similar to [9], it still needs additional circuit components to realize the sum and difference of the two input signals i_x and i_y ($i_x + i_y$ and $i_x - i_y$). The CMOS current multipliers of [11] were realized by using a pair of voltage-translinear loops of MOS transistors. Their important features are simplicity, precision and wide dynamic range. However, the circuits were biased by the dc supply voltages of 5 V and 3 V, which result in high power consumption. Basically, the circuit operation at low-voltage level is a common practice adopted to reduce total power consumption.

For a typical *n*-well CMOS process, the transition frequency f_t of NMOS transistor is approximately two times higher than the f_t of PMOS transistor, because electrons have a higher saturation velocity compared to holes [12]. In addition, to realize the same transconductance with transistors of the same gate length, a PMOS gate length must be three times wider than a NMOS. This is due to the fact that the junction capacitance per unit area is approximately two times larger for PMOS than for NMOS [13]. Therefore, the circuit design technique in which all small-signals pass through only NMOS transistors is preferable for a high frequency of operation [14].

This paper proposes a simple four-quadrant current-mode analog multiplier based on the famous current squaring circuits [15, 16]. The circuit is designed by employing 19 NMOS transistors and 8 bias current sources, where the small-signal paths are realized through only NMOS devices. Since only two NMOS transistors and one bias current source are stacked between positive supply voltage and ground, the proposed multiplier circuit can be operated at the low-voltage level. To demonstrate the proper circuit operations, computer simulation results based on TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm CMOS technology with a single 1.5 V supply voltage have been provided.

2. BASIC PRINCIPLE

The basic principle of a four-quadrant current-mode multiplier utilized in this work is based directly on the following quadratic relation :

$$i_{out} = (i_x + i_y)^2 - (i_x^2 + i_y^2) = 2i_x i_y \quad , \tag{1}$$

where i_x and i_y are the input current signals, and i_{out} is the output current signal. To realize the current multiplication of eq.(1), the current summing, subtracting and squaring circuits are normally required. It is to be noted that the sum and difference of the current signals can be achieved simply by using the current mirror circuits. The sum-squared and squaring of two currents i_x and i_y can also be achieved by the current squarer circuits, which will be described briefly in the following section.

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3. CURRENT-SQUARING FUNCTION CIRCUIT

Figure 1 shows a current squaring circuit (M_1-M_3) based on the square-law characteristic of MOS transistors in saturation [15, 16]. The bias voltage V_B is supplied by a current-controlled biasing circuit (M_{B1}-M_{B2}), where I_B is the bias current. Assumed that all NMOS transistors are identical and operate in the saturation region, the expression describing its squaring function is shown below.

$$i_o = 2I_B + \frac{i_i^2}{8I_B} \quad . \tag{2}$$

In order to keep the circuit operating properly, the input current i_i must be restricted within the following range :

$$|i_i| < 4I_B \quad . \tag{3}$$

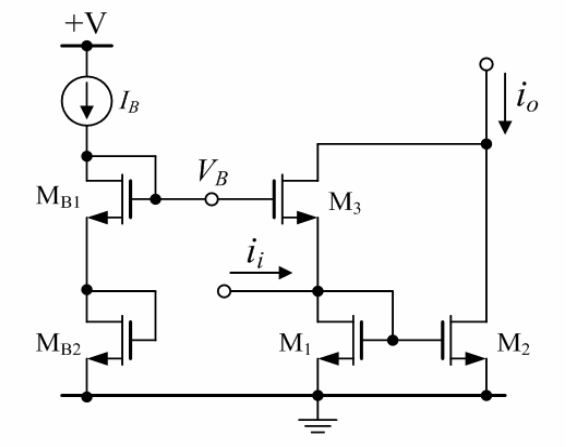

Fig. 1 – Current squarer cell.

4. PROPOSED CURRENT MULTIPLIER CIRCUIT

A complete schematic of the proposed four-quadrant current multiplier is shown in Fig. 2. It is comprised of only 19 NMOS transistors and 8 bias current sources. Transistors M_{1A}-M_{3A}, M_{1B}-M_{3B} and M_{1C}-M_{3C} function the current squaring circuits corresponding to those shown in Fig. 1. To contribute the low power consumption, three current squarers share the biasing circuit (M_{B1}-M_{B2} and I_B). Transistors M_{4A}-M_{6A} and M_{4B}-M_{6B} behave the dual-output current mirrors to generate the *x* input and *y* input current signals (i_x and i_y) and the sum of i_x and i_y ($i_x + i_y$) to the squarer cores. According to eq. (2), the output currents i_{o1} and i_{o2} of the squaring circuits in Fig. 2 are given by, respectively, :

$$i_{o1} = 4I_B + \frac{(i_x^2 + i_y^2)}{8I_B} \tag{4}$$

and

$$i_{o2} = 2I_B + \frac{(i_x + i_y)^2}{8I_B} \quad . \tag{5}$$

Transistors M_7-M_8 form the negative current mirror used to provide an output current i_{out}, which is represented by the difference of the currents i_{o2} and i_{o1} ($i_{out} = i_{o2} - i_{o1}$). Accordingly, from eqs.(4) and (5), the resultant output current (i_{out}) of the proposed multiplier can be expressed by:

$$i_{out} = -2I_B + \frac{i_x i_y}{4I_B} \quad . \tag{6}$$

Equation (6) represents that the circuit of Fig.2 works as the four-quadrant current multiplication between i_x and i_y with the dc output offset current of $-2I_B$. This offset current can be eliminated by adding the dc current source at the output terminal.

In addition, the input resistances at the *x* input and *y* input terminals can be found to be :

$$R_{in} = \frac{1}{2\sqrt{KI_B}} \quad , \tag{7}$$

where $K = \frac{\mu_n C_{ox}}{2}\frac{W}{L}$ is the transconductance parameter of NMOS transistor, μ_n is the electron mobility, C_{ox} is the gate capacitance per unit area of the gate oxide, *W* and *L* are the channel width and channel length of the NMOS, respectively.

5. PERFORMANCE ANALYSES

5.1. INPUT CURRENT MISMATCH

Since the proposed current multiplier circuit of Fig.2 requires two input current signals i_x and i_y, the harmonic distortion may be appeared at the output of the circuit if they are mismatched. Concerning the input current mismatch, they can be modeled as :

$$i_{xi} = i'_x + \Delta_{xi} i'_x \tag{8}$$

and

$$i_{yi} = i'_y + \Delta_{yi} i'_y \quad , \tag{9}$$

where i_{xi} and i_{yi} (i = 1, 2) are the nominal values, and Δ_{xi} and Δ_{yi} are the mismatch percentages of i_x and i_y, respectively. In this case, we assume that the currents i_{x1}, i_{y1} and (i_{x2} + i_{y2}) are injected to M_{1A}, M_{1B} and M_{1C}, respectively.

A calculation using eqs.(8) and (9) gives the output current due to input-current mismatching effect as the following expressions :

$$i_{out} = -2I_B + \frac{2\alpha_{xy}(i'_x i'_y) + \alpha_x (i'_x)^2 + \alpha_y (i'_y)^2}{8I_B} \quad , \tag{10}$$

where $\alpha_{xy} = 1 + 2(\Delta_{x2} + \Delta_{y2})$,

$\alpha_x = (2 + \Delta_{x2})\Delta_{x2} - (2 + \Delta_{x1})\Delta_{x1}$,

and $\alpha_y = (2 + \Delta_{y2})\Delta_{y2} - (2 + \Delta_{y1})\Delta_{y1}$.

Suppose i'_y is kept constant equal to I_{my}, and i'_x is the sinusoidal signal with the following form : $i'_x = I_{AC} \cos \omega t$, where I_{AC} is a peak amplitude of the sinusoidal signal. From eq.(10), the generalized second harmonic distortion (HD_2) with respect to the input signal can be derived as [16–18]:

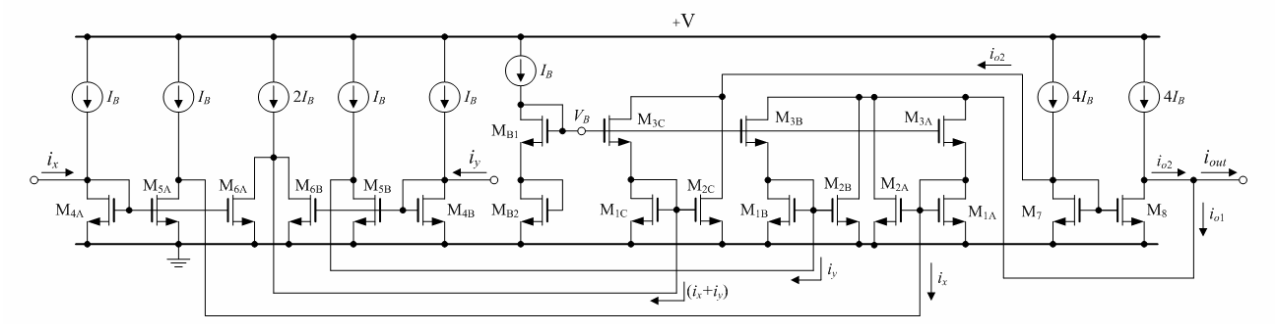

Fig. 2 – Proposed NMOS-based four-quadrant current multiplier.

$$\mathrm{HD}_2 = \frac{[(2+\Delta_{x2})\Delta_{x2} - (2+\Delta_{x1})\Delta_{x1}]I_{AC}}{4[1+2(\Delta_{x2}+\Delta_{y2})]I_{my}} \quad . \tag{11}$$

This result shows that the input current mismatch produces second harmonic distortion in the output current obviously. For example, for typical set of device parameters with $|\Delta_{xi}| \le 1$ % , $|\Delta_{yi}| \le 1$ % and $I_{AC} = I_{my}$, the worst-case estimate of HD_2 introduced by the input current mismatch is therefore about 1 %.

5.2. TRANSCONDUCTANCE PARAMETER MISMATCH

The other essential non-ideality contributing to harmonic distortion is the mismatch in the transconductance parameter (K) of the saturated transistors. To consider this situation, it is assumed that the transconductance parameter mismatch in NMOS transistor may be modeled by :

$$K_j = K' + \delta_j K' \quad , \tag{12}$$

where K' and δ_j are the nominal value and the mismatch percentage of K of M_j, respectively. Using the same derivation as above, the HD_2 caused by the transconductance parameter mismatch can be approximated as :

$$\mathrm{HD}_2 = \left[1 - \frac{(1+\delta_{1C})(1+\delta_7)}{(1+\delta_{1A})(1+\delta_8)}\right]\frac{I_{AC}}{2I_{my}} \quad . \tag{13}$$

Equation (13) suggests that the mismatch of K seems to generate second harmonic distortion. Also, using the same parameters as mentioned before, a typical 1 % mismatch in K-value results in less than 1 % HD_2.

5.3. THRESHOLD VOLTAGE MISMATCH

In practice, the threshold voltage V_T of NMOS transistors is changed by the bulk voltage or the source-substrate voltage V_{SB}, which is the so-called body effect. Usually, V_{SB} is not equal to zero so that the body effect must be taken into consideration. Therefore, including this effect, the threshold voltage for NMOS devices can be defined as :

$$V_{Tj} = V'_T + \beta_j V'_T \quad , \tag{14}$$

where β_j represents the percentage variation of V_T of M_j with respect to its nominal value V'_T. Using the defining relation of (14), the output current deviation from that given in eq.(6) will be obtained as :

$$\Delta i_{out} \cong [4\beta_T \sqrt{KI_B} + (\beta_7 - \beta_8)^2 V'_T K].V'_T \quad , \tag{15}$$

where $\beta_T = \beta_{1A} + \beta_{3A} + \beta_{1B} + \beta_{3B} + \beta_{1C} - \beta_{3C} - 2\beta_B$. (16)

It is evident that the threshold voltage mismatch leads to a dc offset current, which directly proportional to the bias current I_B. Thus, this offset current can be regarded as an error in the bias currents of the multiplier, and in practice can be compensated by slightly adjusting them from their theoretical values.

5.4. BANDWIDTH LIMITATION

There are two major dominant poles that restrict the operating frequency of the proposed multiplier circuit of Fig. 2. One is the parasitic pole of the squaring circuits and the other is the dominant pole associated with the current mirrors. By referring to the squaring circuits M_{1k}-M_{3k} (k = A, B, C) in Fig.2, and assuming that $K_j = K_{j\mathrm{A}} \cong K_{j\mathrm{B}} \cong K_{j\mathrm{C}}$ and $C_{gsj} = C_{gsj\mathrm{A}} \cong C_{gsj\mathrm{B}} \cong C_{gsj\mathrm{C}}$, where C_{gsj} is the gate-to-source junction capacitance of M_{jk} (j = 1, 2, 3), the approximate parasitic pole ω_{p1} of these circuits can be predicted as :

$$\omega_{p1} \cong \frac{2\sqrt{I_B}\left(\sqrt{K_1} + \sqrt{K_3}\right)}{C_{gs1} + C_{gs2} + C_{gs3}} \quad . \tag{17}$$

Consider the current mirrors M_{4A}-M_{6A} and M_{4B}-M_{6B} in Fig. 2. In the same manner, equal transconductance parameters and gate-to-source junction capacitances are assumed for similar devices. Then, the second parasitic pole ω_{p2} introduced by these simple current mirrors can be determined by :

$$\omega_{p2} \cong \frac{2\sqrt{K_4 I_B}}{C_{gs4} + C_{gs5} + C_{gs6}} \quad , \tag{18}$$

where $K_4 \cong K_{4\mathrm{A}} \cong K_{4\mathrm{B}}$.

In avoid the parasitic pole influences arising from squarer and mirror circuits, the maximum operating frequency must be less than ω_{p1} and ω_{p2}. As a consequence, the useful bandwidth of the proposed multiplier circuit in Fig.2 can be defined simply as :

$$\omega << \min\{\omega_{p1}, \omega_{p2}\} \quad . \tag{19}$$

6. COMPUTER SIMULATION AND VERIFICATION

To confirm the analytical expressions given above, the proposed circuit of Fig.2 has been simulated using PSPICE program with TSMC 0.35 μm CMOS technology. The supply voltage was $+V$ = 1.5 V and the bias currents I_Bs were set to 40 μA. The aspect ratios of NMOS transistors constructing in the proposed circuit of Fig.2 are given in Table 1.

Table 1

Transistor aspect ratios of the proposed current-mode multiplier of Fig. 2

Transistors	*W/L* (μm/(μm)
M_{1A} - M_{3A}, M_{1B} - M_{3B}, M_{1C} - M_{3C}, M_{B1} - M_{B2}, M_{4A} - M_{4B}	16.1/0.35
M_{5A}, M_{5B}	16.8/0.35
M_{6A}, M_{6B}	16.5/0.35
M_7 - M_8	3.5/0.35

Figure 3 shows the simulated DC current transfer characteristics of the proposed four quadrant current multiplier of Fig. 2, showing i_{out} against i_x with i_y as a parameter. For an input range up to ±40 μA, the proposed multiplier has good linearity with the nonlinearity error of less than 2 %. From the simulation results, the static power consumption (@ $i_x = i_y$ = 20 μA) was about 0.98 mW, and the measured corresponding –3dB bandwidth (BW) was up to about 10 MHz. This multiplier has an input referred noise current of about 28 pA/(Hz)$^{1/2}$. To evaluate the distortion performance of the circuit, the dc current with the peak amplitude of 20 μA was applied to the y input (i_y = 20 μA), while the 100 kHz sinusoidal current signal i_x was injected to the x input. The simulated total harmonic distortions (THDs) of i_{out} as a function of the i_x/I_B ratio are plotted in Fig.4. The plots demonstrate that the input current amplitudes as large as 40 μA lead to THD values lower than 2.5 %. The important performance parameters of the proposed current multiplier of Fig. 2 are summarized and compared with the similar available works [4–11] in Table 2.

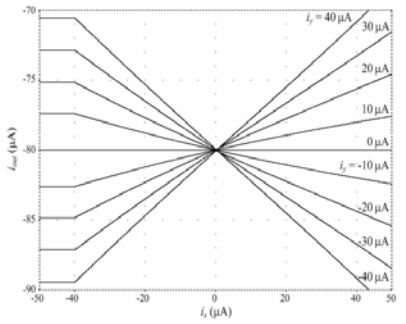

Fig. 3 – Simulated dc current transfer characteristics of the proposed multiplier in Fig.2.

Table 2

Performance comparison between the proposed current-mode multiplier of Fig. 2 and the other works cited [4–11]

Multipliers	NMOS only	Input current range	Static power consumption	–3dB BW	THD	Input referred noise current	Supply voltage	Technology
[4]	no	N/A	N/A	N/A	N/A	N/A	±4 V	SPICE3C1 level 3
[5]	no	±50 μA	N/A	66 MHz	N/A	N/A	±3.3 V	N/A
[6]	no	±10 μA	340 μW	42 MHz	0.97%	N/A	+3.3 V	BSIM3v3 0.35 μm
[7]	no	±2 μA	N/A	N/A	N/A	N/A	±0.75 V	0.8 μm
[8]	no	±100 nA	9 μW	19 MHz	< 1% (@ 100 nA_p, 100 kHz sinusoid)	N/A	+2 V	0.35 μm
[9]	no	±60 μA	671 μW (@ $i_x = i_y$ = 0 μA) 720 μW (@ $i_x = i_y$ = 60 μA)	31 MHz	4.485% (@ 50 μA_p, 1 MHz sinusoid)	46 pA/(Hz)$^{1/2}$	±1.5 V	0.5 μm
[10]	no	±15 μA	184 μW	5.5 MHz	0.9% (@ 12 μA_p, 1 kHz sinusoid)	N/A	+1.5 V	0.8 μm
[11]	no	0-100 μA	700 μW	12.3 MHz	1% (@ 20 μA_p, 10 kHz sinusoid)	N/A	+5 V	MIETEC 2.4 μm
			600 μW	3 MHz	1.5% (@ 20 μA_p, 10 kHz sinusoid)		+ 3.3 V	
Proposed circuit	yes	±40 μA	960 μW (@ $i_x = i_y$ = 0 μA) 980 μW (@ $i_x = i_y$ = 20 μA)	10 MHz	< 2.5% (@ 40 μA_p, 100 kHz sinusoid)	28 pA/(Hz)$^{1/2}$	+1.5 V	TSMC 0.35 μm

N/A : not available

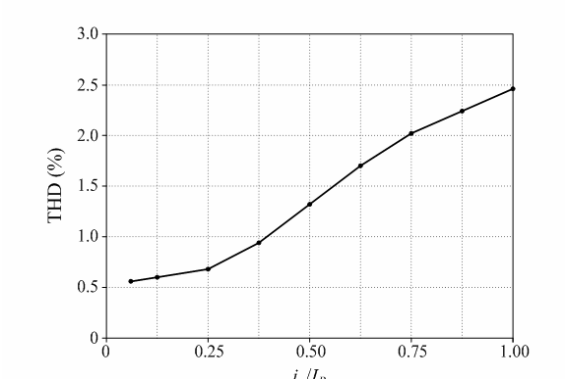

Fig. 4 – THD of i_{out} versus the ratio of i_x/I_B with f = 100 kHz.

As a particular example of the circuit versatility, the proposed multiplier was used to implement the frequency doubler, i.e. $i_x = i_y$. In this case, $i_{in} = i_x = i_y = 40 \sin(2\pi\times10^4 t)$ μA is chosen for frequency doubling. Fig. 5 shows the simulated input and output waveforms of the proposed current multiplier acting as a frequency doubler, and the frequency spectrum of i_{out} is also shown in Fig. 6. One can verify that the output current is a sinusoidal signal of twice the input signal frequency. As expected, the offset of the circuit is about 80 μA. The THD of i_{out} was also evaluated and its value remains under 1.28 %, a small value.

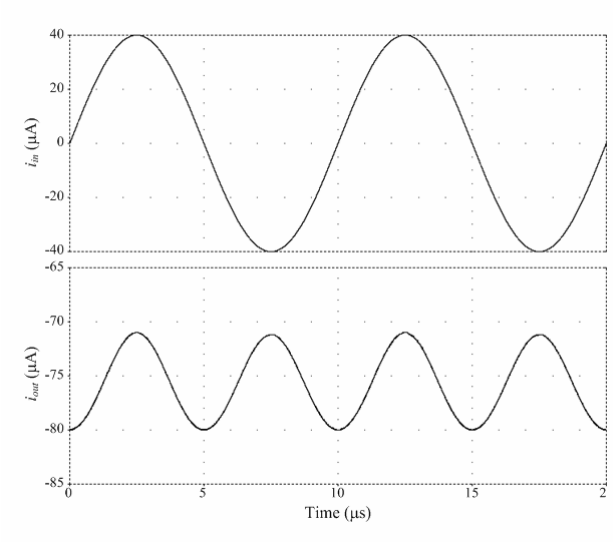

Fig. 5 – The proposed current multiplier as a frequency doubler.

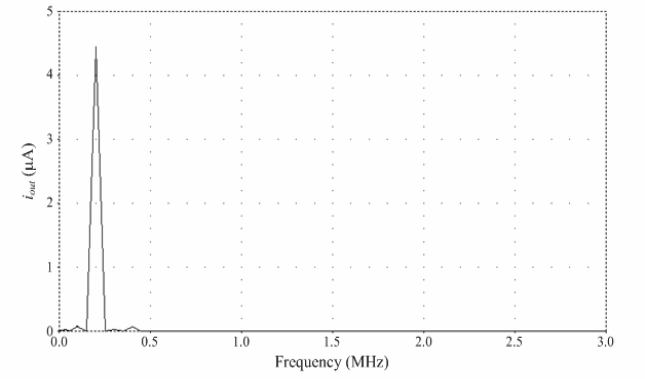

Fig. 6 – Frequency spectrum of i_{out} when acting as a frequency doubler.

Other application of the proposed multiplier as an amplitude modulator has also been tested. In this way, two current signals i_x and i_y were applied to the circuit of Fig. 2. The current i_x is a 10 kHz sinusoidal modulating signal of 40 μA (peak), while the current i_y is a 100 kHz sinusoidal carrier of 40 μA (peak). Figure 7 demonstrates the simulated performance of the proposed multiplier when functioning as a modulator.

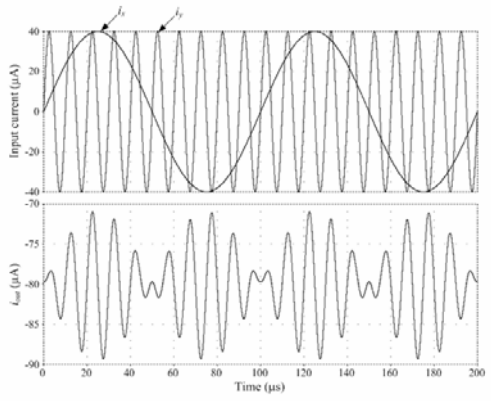

Fig. 7 – The proposed current multiplier as a modulator.

7. CONCLUSIONS

The objective of this paper is to present the simple realization of the four-quadrant current-mode multiplier circuit based on current-squaring function circuits using all NMOS transistors. Since it is designed where all small-signal currents are realized by using only NMOS transistors, the resulting circuit can be used in low-power, low-voltage and high-frequency applications. Simulations based on TSMC 0.35 μm CMOS process parameters are performed. Specifications achieved include low-single supply voltage (+ 1.5 V), low power dissipation (< 0.98 mW), THD of < 2.5 % for 40 μA peak and linearity error of < 2 %.

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