MODELLING THE ELECTROSTATIC DISCHARGE PHENOMENA OF A CMOS ADDER STRUCTURE

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This paper deals with diagnosing the failure effects in applying electrostatic charges on a model based on MOSFET transistors. In this regard, the work highlights the performance of a One-bit full adder CMOS structure by applying high stresses on one of its inputs. The testing results are carried out using the CADENCE IC 5.3 software package by considering the alternative electrostatic discharge implementation of the transmission line pulse method. The functionality of the structure was improved by adding several electronic components with electrostatic discharge protective properties.

1. INTRODUCTION

For the past decades, the downscaling of the transistor dimensions in CMOS technologies has ensured higher packing density, higher performance and lower cost of integrated circuits [1].

In the process of CMOS technology scaling there are several factors with major impact in achieving a good functionality and a high performance of the devices. For example, in the presented paper Parameter variations and impact on circuits and microarchitecture, Borkar et al. emphasize the role of the parameter variation in estimating the performance of the devices. In their paper, they review that the within-die variations arise either from environmental variations: temperature, voltage supply or from physical process variations: channel length, oxide thickness, random dopant fluctuation [2].

The constant evolution of the CMOS semiconductor technology determines also an increase of malfunction circuits due to the electrostatic discharge (ESD) events. The process in which the static charge is dissipated to the topology of the integrated circuits highly affects the integrity of the devices. Rajashree Narendra

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et al. confirm that the static charge is represented as a high voltage, giving rise to a high peak current which usually causes the breakdown of an insulating oxide transistor layer or even the burnout of the device [3]. The breakdown of the gate oxide and the increase of the leakage paths are the main factors that determine the ESD degradation of the devices.

In terms of ESD issues, the ESD Association (ESDA) has been focused on advancing the theory and practice of the electrostatic discharge phenomenon, its scientific publications representing the state of art of this research area. The association installed working groups trained on implementing comprehensive ESD electronic design automation verification by investigating the leakage current flows in modern integrated circuits [4–7].

The integrated devices are qualified for their built-in reliability according to the well-known standards: human body model [5], machine model [6] and charged device model [7]. Another stressing method related to the classical component level ESD models (HBM, MM) used in ESD device characterization is the transmission line pulse technique.

This paper presents the computational analysis of the one-bit full adder CMOS structure for current issues in the electrostatic field regime. A new approach in evaluating the effects of the high currents is proposed in this paper.

This approach relies on the transmission line pulse (TLP) model, the most improved semiconductor ESD test method.

2. ONE-BIT FULL ADDER CMOS MODEL

In this section the functionality of the CMOS structure is discussed. The basic arithmetic block of the one-bit full adder has three one-bit inputs: the bit of $A$, the bit of $B$ and the carry in bit: $C_{in}$ which generates two one-bit outputs, typically represented by the signals of the sum bit: $SUM$ and the carry out bit: $C_{out}$. The outputs of the circuit: $SUM$ and $C_{out}$ are calculated based on the following logical expressions:

$$SUM = C_{in} \oplus A \oplus B, \quad (1)$$

$$C_{out} = (A \& B) + C_{in}(A \oplus B) = (A \& B) + (A \& C_{in}) + (B \& C_{in}), \quad (2)$$

where & represents the logical AND operator, + the logical OR operator and $\oplus$ the logical XOR operator.

The $SUM$ output is TRUE, when the $A$, $B$ and $C_{in}$ have an odd number of bits; the carry out: $C_{out}$ is TRUE when $A$ and $B$ are TRUE or when $C_{in}$ is TRUE and $A \oplus B$ is TRUE.
The characterization of the arithmetic block is carried out using a schematic model implemented in 0.18 µm CMOS technology based on CADENCE IC 5.3 software package (Fig. 1).

The implementation of the one-bit full adder (1-bit FA) diagram combines PMOS pull-up and NMOS pull-down networks (in a number of 28 MOSFET transistors) using AND, OR and XOR logical gates.

The current waveforms of the 1-bit FA simulations are illustrated in Fig. 2.

3. TESTING METHOD

A powerful tool in providing consistent information about the semiconductor behavior is the transmission line pulse (TLP) electrostatic discharge method. The transmission line pulse testing method provides the ability to measure the current/voltage characteristics of the devices in terms of electrostatic discharge issues (high currents, short duration pulses, fast rise/fall times, breakdown effects). The transmission line pulse is a model widely used in the test field for analyzing the behavior of a device, when it is exposed to an ESD event [8].

The introduction of TLP has enabled designers to reconsider the failures occurring in the circuits due to the ESD events. Keppens et al. consider that the most reliable failure criterion for device characterization is the "detection of any
change in leakage current” [9]. An increase in leakage of $I_{\text{leakage}} > 10 \, \mu\text{A}$ may imply signs of device limitations [10].

4. ANALYSIS OF THE TLP ESD TEST

The process in which the static charge is dissipated to the topology of the integrated circuits was highly investigated by the scientific community in order to establish the proper ESD standard procedures. All the standards are developed and maintained by standardization committees of international organizations. The EN 61000-4-2, corresponding to the IEC 61000-4-2 [11], qualifies the operation of the system under test, the stress levels and the possible system response.

The correlation between TLP and HBM/MM has been studied extensively, yielding theoretically and empirically derived correlation waveforms [12].

The equivalent circuit of the transmission line pulse model is implemented in Fig. 3. The testability using the TLP method consists in discharging a transmission line on a device under test, generating square waveforms. As corresponding to the IEC 61000-4-2 standard, the ESD HBM testing is realized using a resistance of 2 Ω as device under test. In order to observe the similarities between the HBM and TLP ESD stress methods, the previous TLP simulation is realized having the same device under test as the one used in the HBM testing.

The stress levels applied in the discharge methods using cables as transmission lines are usually significantly higher than the ESD standard stress levels. The manner in which semiconductor devices behave in such harsh conditions represents a challenge to be investigated. As a matter of fact, the transmission line will be charged using high impedance at a high voltage supply (25 kV) and hereby discharged on the test device. The high voltage supply controls the current waveform amplitude. The transmission line length sets the pulse duration.

The pulse length $\tau_{TLP}$ of the transmission line is described by:

$$\tau_{TLP} = \frac{2L_{TLP}}{\nu} \sqrt{\frac{1}{\mu\varepsilon}}$$

with $\nu$ propagation velocity, $L_{TLP}$ the transmission line length of cable, $\mu$, the relative permeability and $\varepsilon$, relative permittivity.

Knowing that the parameters of the transmission lines have a high influence on the discharge current waveform, for the simulations it is considered a cable of 50 Ω characteristic impedance, 4 m length and a propagation velocity of 66. According to the length dimension, the pulse width is in the range of approximately 40 ns per meter cable length.
For a 25 kV stress voltage, the TLP tester injects a current up to about 80 A into DUT. The 50 Ω resistor \( R_L \) provides a controlled load for the transmission line. In this process of testing, an attenuator adjusts the voltage level that DUT receives and prevents from reflecting off the transmission line and returning an extra energy to the DUT. The main advantage of the attenuator consists in maintaining the pulse-shape not altered. Removing the attenuator causes the current pulse to be reflected to the DUT and back to the power supply, where it finds a high impedance source. Further, the current pulse is reflected back again to the transmission line and back to DUT, with polarity inverted. In this case the accuracy of the measurements is distorted by the reflections of the signal. In Fig. 4 are represented the current waveforms of the TLP testing in the case of using an attenuator and without it.

![Fig. 3 – Characteristic circuit for the transmission line pulse model.](image)

![Fig. 4 – a) Current waveform of the TLP; b) reflected current waveform of the TLP.](image)

The corresponding waveform of the TLP differs from the standardized ESD waveforms by means of rise time, delay time, pulse width, amplitude. Basically, TLP it is a pulsed method having complete different stress levels than the HBM/MM standards; practically it is a different failure mechanism.

The reflected waveform illustrated in Fig. 4 is described in terms of pulse reflections, through the reflection coefficient for each lobe amplitude [13]:

\[
\sigma_{L,i} = \frac{V_{r-i}}{V_{f-i}} = \left( \frac{V_{br}}{V_r} \right) \frac{Z_0}{R_{dynamic} + Z_0} + \frac{R_{dynamic}}{R_{dynamic} + Z_0},
\]

(4)

where the following notations are used: \( V_{r-i} \) and \( V_{f-i} \) for the forward/reverse voltage waveform reflections, \( V_{br} \) for the breakdown voltage of the DUT and \( R_{dynamic} \) for the dynamic resistance of the DUT at breakdown.
Knowing that the gate oxide thickness represents a critical parameter of the transistors in CMOS technology, in this paper the TLP stress is applied on a structure using MOSFET transistors. Therefore, a high voltage source delivering enough power stresses the $A$ input of a 1-bit Full Adder cell (Fig. 5). The following tests are realized for the same parameters of the transmission line as the ones used below. The rise time of 700 ps is used for having fast transitions. The waveforms of the TLP tests applied on the FA structure are illustrated in Fig. 6. The discharge occurs during the transmission of ones of the data stream.

The degradation of the output waveforms shows the circuit malfunction during the ESD event. The data outputs are being affected by the high impulse coming from the charged transmission line.

The ESD transients influence the amplitude of the output data, affecting the ones and the zeros of the data stream and also introduce a delay of the data.

In order to alleviate the ESD effects is considered the solution of using several components with protective properties. The protective structure consists in the following components:

- shunt devices to discharge positive polarity transients,
- shunt devices to discharge negative polarity transients,
- series elements for current limiting.

In the designed protection circuit, the clamping diodes shunt the transient current to the safe levels, the power supply line $V_{dd}$ or the ground. A positive transient voltage determines $D_1$ diode to be forward biased when the input voltage exceeds $V_{dd}$. Similarly, for negative transients, $D_2$ diode shunts the negative current. The diodes are used due to the small junction capacitance, which has a less impact on the bandwidth of the circuits [15]. In order to sustain a high ESD level, the design should have ESD clamp devices in a reasonable area to sustain a high-enough ESD level [14, 15].

The resistors serve to limit the peak current of the ESD pulses. The $R_{p1}$ and $R_{p2}$ resistances protect the inputs of the device, by limiting the ESD current flowing. In this regard, the value of $R_{p1}$ resistance (25 kΩ) is chosen larger, to reduce the high current.

The $R_{p2}$ resistance is smaller, having 688 Ω. This value was considered taking into consideration the fact that the large series resistance and the large junction capacitance of ESD clamp devices cause a long resistance – capacitance ($RC$) delay to the input signals [16].
Fig. 5 – TLP testing of the 1-bit FA test circuit and the protection structure considered.

Fig. 6 – Comparison between the test waveforms of the transmission line pulse ESD stresses:
   a) TLP tests of the 1-bit FA; b) TLP tests using a protection structure;
   c) TLP tests using protection and introducing delays to the input data.
The use of the protection structure eliminates the bad ESD transients on the amplitude of the output data $C_{out}$ and $SUM$, reducing the current corresponding to the A input, $I_A$ to 5.2 A. In order to maintain the adder function, the current values of the $B$ and $C_{in}$ inputs are modified to 5.2 A. The ESD transient also affects the proper functioning of the circuit by introducing a short delay to the A input data and its effects are observed. A short delay of about 3.86 ns is introduced at the A input data which implies the distortion of the output data transmission, affecting the ones and zeroes of the data.

In order to eliminate the problem of disturbing the order of transmitting the bits for the $C_{out}$ and $SUM$ data outputs, delay times (of 3.86 ns) are applied for $B$ and $C_{in}$ inputs. These times are applied by introducing the 3.86 ns values to the delay parameters in declaring the voltage sources of the two inputs. As shown in Fig. 6, the set of data [01101001] for $SUM$ and [00010111] for $C_{out}$ are not disturbed anymore.

This study aims to highlight the main failure effects related to the electrostatic discharges and the manner in which can be reduced.

In conclusion, it is observed that when the transient is discharged during the transmission of ones, the amplitude of the data is affected and also the order of the transmission of the bits is distorted. The use of a protection structure eliminates the amplitude issues and reduces the current flow. Also, resizing the current values and the delay times of the $B$ and $C_{in}$ sources implies a valid reproducing in the transmission of data bits.

4. CONCLUSIONS

The malfunction of a 1-bit FA CMOS structure due to the effects of an electrostatic field resulting in bad transients introduced in the data stream is investigated.

It has been observed that the ESD event affects the amplitude of the signal, resulting in distorted waveforms. Also, the ESD transient introduces a delay to the input data which affects the ones and zeroes of the output data.

By using the protection scheme, the ESD built-in reliability of the circuit giving the data stream has been improved by eliminating the amplitude failures.

The effect of applying delay times to the $B$ and $C_{in}$ inputs determines a good functionality of the adder circuit.

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