COMPARISON BETWEEN FIVE-LEVEL FLYING CAPACITOR STRUCTURES

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Abstract. In the paper is presented a comparison between two five level converters in view of total power losses in the semiconductor devices and the parameters of the output voltage. The two structures use the flying capacitor concept and are derivative from three level topologies. These structures are presented and discussed in order to describe how the five level versions were obtained and why. Simulation and experimental results are presented in order to verify the theoretical studies made.

1. INTRODUCTION

Multilevel conversion structures represent a solution to improve the performances given by the classical structures with two voltage levels. Building high voltage semiconductor devices present technical difficulties. Multilevel structures offer a reduction of the voltage stress that compensates for the increased number of devices.

The development of these structures began with the solution given by Bhagwat in 1980 called Stack Cell Converter (SC) [1]. This solution gave a reduction to half of the voltage stress in the semiconductor devices but had the disadvantage of an unequal loss distribution that represented a limitation to the maximum output power that could be achieved. In order to solve this problem, several multilevel structures were developed. Among them the most utilized in industrial applications is the Neutral Point Clamped Converter (NPC) because of the low number of devices used comparative with the other structures [2]. This structure was followed by the Active Neutral Point Clamped Converter (ANPC) developed by Bruckner in 2001. It presents the advantage of an increased number of degrees of freedom [3, 4].

An important class of multilevel structures is represented by the structures that use the Flying Capacitor concept (FC) [5]. This class of structures has the...
advantage of increasing the apparent switching frequency which leads to a decrease in the output filter. At high switching frequency, the flying capacitor has a small size and the overall performances are better compared to other type of structures. The additional expense of the flying capacitors, particularly at low and moderate switching frequencies is the main disadvantage of the FC topologies. Because the classical multilevel structures without the flying capacitor concept offered good results at a low switching frequency, there were created solutions that combine the two concepts [6]. Increasing the number of voltage levels leads to a better output voltage waveform and to a lower output filter.

This paper presents two five-level structures, the 5L-AVNPC (Active Vienna Neutral Point Clamped) converter [7] and the 5L-ANPC-FC (Flying Capacitor ANPC) [8] that use the flying capacitor concept and are derivative from three-level converters. The features of the three level converters are presented in order to create the translation to the five-level structures.

Analytical methods to estimate the power losses in the semiconductor devices are described and their results are used to compare the two structures. Also the comparison is made regarding the total harmonic distortion factor (THD) and the efficiency of the power conversion. While most papers present the power losses for each device at a modulation index (M) close to one for inverter operation [9], this work presents results for a small modulation index. This situation appears in low speed applications.

This paper is organized as follows. The operation mode and features for the 3L-AVNPC, 3L-ANPC and 3L-FC converters are presented in section II. The translation to five-level conversion and the resulting operation and control is presented in section III. Section IV contains a theoretical method to estimate the power losses in the semiconductor devices. Section V contains the comparison between the two structures and the presentation of the results from an experimental test bench. Finally conclusions and references are given.

2. THREE LEVEL STRUCTURES

The five-level structures were developed in order to improve on the characteristics given by the three-level topologies. These structures with three voltage levels are presented along with their features.

The 3L-ANPC (Active Neutral Point Clamped) converter is derivative from the NPC converter having two active switches placed in anti-parallel with the clamped diodes (Fig. 1a). This converter have more degrees of freedom compared with the previous structures from this class and allows using more control methods in order to obtain various power loss distributions and output characteristics [3]. Each device supports a voltage equal to half of the supply voltage.
The 3L-FC (Flying Capacitor) converter is made from four Insulated Gate Bipolar Transistors (IGBT) and one capacitor (Fig. 1b). Instead of using clamped diodes as it was the case for the 3L-NPC structure, the FC structure uses clamped capacitors. This structure presents the advantage of a reduced capacitor size and good properties for the output voltage at a high switching frequency.

The 3L-AVNPC (Vienna ANPC) converter was first presented in [7] as an inverter based on the Vienna rectifier structure (Fig. 1c). The Vienna rectifier was made from six diodes and one transistor. In the 3L-AVNPC inverter six bidirectional devices replace the six diodes from the basic structure. From the seven transistors, only three operates at the frequency of the carrier wave, the rest being used at the frequency of the reference wave. The transistor $S_{1C}$ is connected between the points C and D from the 3L-ANPC structure and it is used as a shared device between the two high frequency commutation cells. For the inverter operation mode the load current does not pass through the shared device, making this solution best suited for low speed applications.

With the increase of the number of voltage levels the quality of the output voltage increases and the stress on the semiconductor devices is reduced. This property allows the use of lower voltage devices and therefore the operation at a higher switching frequency. At a low switching frequency the flying capacitor is expensive and the global performances are worse compared with the structures that do not use the flying capacitor concept. For these reasons, the five-level solutions present interest and will be presented in the next section.

Fig. 1 – Three level structures:
a) 3L-ANPC; b) 3L-FC; c) 3L-AVNPC.
3. FIVE LEVEL STRUCTURES

3.1. FIVE-LEVEL ACTIVE NEUTRAL POINT CLAMPED FLYING CAPACITOR CONVERTER

The combination between the 3L-ANPC converter and the 3L-FC converter results in the five-level structure called 5L-ANPC-FC that was first presented in [11]. It is made from eight switches and one flying capacitor (Fig. 2a).

The eight transistors are complementary controlled: S1-S1C, S2-S2C, S3-S3C and S4-S4C. The PWM control is made by using four carrier waves ($C_x$, $x = 1$ to 4) shifted on both axis compared with a sinusoidal reference wave (S) (Fig. 2b). The devices $S_3$-$S_{3C}$ and $S_4$-$S_{4C}$ supports a voltage equal to half of the input voltage, form the high voltage stage (HV) and are in conduction on half of cycle. The devices $S_1$-$S_{1C}$ and $S_2$-$S_{2C}$ support a voltage equal to a quarter of the input voltage, form the low voltage stage (LV) and are in conduction on the entire cycle (Fig. 3). The HV devices switch with the frequency of the reference wave which leads to lower losses in commutation. The LV devices switch with the frequency of the carrier wave.

![Fig. 2 – Five-level ANPC-FC converter: a) topology; b) PWM control.](image)

Any switch S is made form a transistor T and an anti-parallel diode D.

The flying capacitor must be charged with a voltage equal to only a quarter of the input voltage ($V_{DC}$), which leads to a small energy stored inside the capacitor. For this reason, this structure has good results even at a low switching frequency compared with other structures that use the flying capacitor concept. The first important harmonic of the output voltage appears at a frequency two times larger than the frequency of the carrier wave.

The main disadvantage of this structure is the unbalanced loss distribution in the LV stage for a modulation index lower than 0.5.
3.2. FIVE-LEVEL ACTIVE VIENNA NEUTRAL POINT CLAMPED CONVERTER

The 5L-AVNPC structure [10] is obtained from the combination between the flying capacitor concept and the 3L-AVNPC converter (Fig. 4). It is made from twelve IGBT devices and two flying capacitors and has a low voltage stage (LV) that supports a quarter of \( V_{DC} \) and a high voltage stage (HV) that supports a half of \( V_{DC} \). The devices of the LV stage commute with the frequency of the carrier wave (HF) and form two classical flying capacitor converters: \( S_{11}-S_{1C}, S_{12}-S_{1C} \) and \( S_{21}-S_{2C}, S_{22}-S_{2C} \).

The devices of the HV stage commute with the frequency of the reference wave. The devices \( S_{1C} \) and \( S_{2C} \) are shared for the two high frequency cells. The transistors \( S_{51} \) and \( S_{61} \) are series connected with \( S_{21} \) and \( S_{12} \) in order to obtain the same voltage stress on all the semiconductor devices from the LV stage. The PWM
control is made by using two positive carrier waves phase shifted with half of switching period compared (Fig. 5) with a modulus reference wave (S_r).

When the reference wave (S) is positive, the switches S_{11} and S_{21} are complementary controlled with S_{1C} and S_{2C}. If the modulation index (M) is smaller than 0.5, the output voltage has three voltage levels: \(-V_{DC}/4, 0, V_{DC}/4\) [Fig. 5 (a)]. If M is larger than 0.5 the other two voltage levels are obtained: \(-V_{DC}/2\) and \(V_{DC}/2\).

When S is negative, the switches S_{12} and S_{22} are complementary controlled with S_{1C} and S_{2C} and the way the voltage levels are obtained remains the same. The diode of the shared devices S_{1C} (D_{1C}) and S_{2C} (D_{2C}) switch at zero voltage if M is smaller than 0.5 and the structure is working in inverter mode (Fig. 6b and c). The apparent switching frequency (f_{ap}) is two times larger than the switching frequency at any modulation index. For all the structures that use the flying capacitor concept it is required to choose a capacitor value that limits the voltage ripple across the capacitor (1).

\[
C_F = \frac{I_{\text{load}} \cdot \sqrt{2}}{\Delta V_F} \cdot \frac{1}{f_{sw}}. \tag{1}
\]

In equation (1), \(I_{\text{load}}\) is the rms value of the load current, \(\Delta V_F\) is the peak-to-peak voltage ripple across the flying capacitor and \(f_{sw}\) is the switching frequency.
4. POWER LOSS ESTIMATION

The temperature of the power devices defines the maximum output power and is dependent on conduction and switching power losses [10]. In order to know the maximum output power it is necessary to estimate the total power loss. This has been done by knowing the thermal and electrical parameters of each device. To obtain this estimation the following simplifying hypothesis were made:

- The output current is sinusoidal.
- The dead time for the transistors is neglected.

4.1. CONDUCTION LOSSES

The conduction losses for an IGBT device can be calculated using a series connection of a DC voltage source representing the on-state zero-current collector-emitter voltage \( u_{CE0} \) and a collector-emitter on state resistance \( r_{C} \) to obtain the dependence between the collector-emitter voltage \( u_{CE} \) and the collector current \( i_{C} \).

\[
 u_{CE}(i_{C}) = u_{CE0} + r_{C} \cdot i_{C} .
\] (2)

The same approximation can be made for the anti-parallel diode (3)

\[
 u_{D}(i_{D}) = u_{D0} + r_{D} \cdot i_{D} .
\] (3)

Using (2) and (3) results the instantaneous value of the conduction losses for the transistor (4) and the anti-parallel diode (5)
\[ p_{cT}(t) = u_{CEq} \cdot i_{C}(t) + r_{C} \cdot i_{C}^2(t), \quad (4) \]
\[ p_{cD}(t) = u_{Dh} \cdot i_{D}(t) + r_{D} \cdot i_{D}^2(t). \quad (5) \]

The average losses in conduction for the transistor (6) and the anti-parallel diode (7) can be expressed using the instantaneous equations (4), (5).

\[ P_{cT}(t) = \frac{1}{T_{sw}} \cdot \int_0^{T_{sw}} p_{cT}(t) \cdot dt = u_{CEq} \cdot I_{Cav} + r_{C} \cdot I_{Cav}^2, \quad (6) \]
\[ P_{cD}(t) = \frac{1}{T_{sw}} \cdot \int_0^{T_{sw}} p_{cD}(t) \cdot dt = u_{Dh} \cdot I_{Dav} + r_{D} \cdot I_{Dav}^2. \quad (7) \]

In equations (6), (7), \( T_{sw} \) is the switching period, \( I_{Cav}, I_{Dav} \) are the average currents for the transistor and diode, while \( I_{Cav}, I_{Dav} \) are the rms currents.

### 4.2. SWITCHING LOSSES

The switching losses for the transistor (\( P_{swT} \)) are dependent on the turn-on energy (\( E_{ON} \)) and turn-off energy (\( E_{OFF} \)) (8). The switching losses for the diode (\( P_{swD} \)) are dependent on the recovery energy (\( E_{REC} \)). These values are obtained from the IGBT datasheet and are a function of the collector current.

\[ P_{swT} = \frac{V_{Tsw}}{V_{CE}} \cdot (E_{ON}(I_C) + E_{OFF}(I_C)) \cdot f_{sw}, \quad (8) \]
\[ P_{swD} = \frac{V_{Dsw}}{V_{CE}} \cdot E_{REC}(I_D) \cdot f_{sw}. \quad (9) \]

In equations (8), (9) \( f_{sw} \) is the switching frequency, \( V_{CE} \) is the collector-emitter voltage, \( V_{Tsw} \) is the voltage switched by the transistor and \( V_{Dsw} \) is the voltage switched by the diode. The output current of each structure is considered to be sinusoidal, a fact that denies a very complex evolution of the dependence between the output voltage and current.

The total power loss in each device represents the sum of the conduction and switching losses for the diode (10) and for the transistor (11).

\[ P_C = P_{cT} + P_{swT}, \quad (10) \]
\[ P_D = P_{cD} + P_{swD}. \quad (11) \]
By using these formulas, the power losses in the presented structures, the 5L-ANPC-FC and the 5L-AVNPC converter were calculated and will be presented in section V.

5. COMPARATIVE STUDY

One of the aspects of this comparative study is the power loss distribution in the semiconductor devices and the total power loss for the two structures considering the inverter operation mode with a power factor PF = 1 for a low speed application (Fig. 7). One of the features of the 5L-AVNPC converter is that some devices switch at zero voltage. Also in order to obtain the \( V_{DC}/4 \) output voltage level the current has two parallel flowing paths: through the transistor of \( S_1 \) and the diode of \( S_{2C} \) or through the transistor of \( S_{21} \) and the diode of \( S_{1C} \). These properties led to a reduction in the power losses compared with the 5L-ANPC-FC structure (Table 1).

The maximum value of the power losses in the semiconductor devices determines the value of the output power for that converter.

![Fig. 7 – Simulated distribution of losses using Eupec FS200R06KL4 IGBT devices \((V_{DC} = 800\, V, f_{sw} = 10\, kHz, M = 0.05, I_{RMS} = 100\, A, PF = 1)\): a) 5L-ANPC-FC; b) 5L-AVNPC.](image)

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<tbody>
<tr>
<td>5L-ANPC-FC</td>
<td>342.3</td>
<td>45.1</td>
<td>387.4</td>
</tr>
<tr>
<td>5L-AVNPC</td>
<td>179.3</td>
<td>34.2</td>
<td>213.5</td>
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The 5L-AVNPC converter uses 50% more devices compared to the 5L-ANPC-FC but the maximum power is increased by 53.7%.

Another comparison parameter is the total harmonic distortion factor (THD) (12). This parameter determines the quality of the output voltage (Fig. 8). The harmonic content decreases with the increase of the modulation index and it is in
average larger with 6.57% for the 5L-AVNPC. The output voltage of the three level structures is less sinusoidal and therefore their THD is greater.

\[
\text{THD} = \sqrt{\sum_{n=3}^{\infty} \frac{V_n^2}{V_1}}. \tag{12}
\]

In equation (12) \(V_1\) is the rms value of the first harmonic and \(V_k\) \((k = 3, 4\ldots n)\) is the rms value of the \(k\)-order harmonic.

The last comparison parameter is the efficiency of the power conversion (13). For the presented structures, the conduction and switching losses were calculated for a modulation index varying from 0.05 to 0.5 taking into consideration the power factor PF=1. In equation (13), \(\eta\) is the efficiency, \(P\) is the total active power, \(P_{\text{CON}}\) represent the conduction losses and \(P_{\text{SW}}\) represent the switching losses.

\[
\eta = \frac{P - (P_{\text{CON}} + P_{\text{SW}})}{P} \times 100. \tag{13}
\]

In average the efficiency for the 5L-AVNPC converter is better with 44.9% compared with the 5L-ANPC-FC converter considering the power factor PF = 1 and a modulation index \(M\) lower than 0.5.

In order to validate the properties of the 3L-AVNPC converter, a low voltage experimental bench was developed, having a RL load with the value of 28 Ω + 20 mH connected between A and O. The PWM control is made by using a field-programmable gate array (FPGA) board. The power devices used, IGBT SKM75GB123D are made by Semikron and rated for 1 200 V and 75 A rms current. The output waveforms are presented (Fig. 9).
6. CONCLUSIONS

This paper presented a comparison between two five level converters. The reason for using five-level structures instead of three-level solutions was presented in section 2. Section 3 presented the two converters with their PWM control and advantages. A theoretical study regarding the estimation of the power losses in the semiconductor devices was presented in section 4. Section 5 presented a comparative study between the two structures made from the point of view of the total power losses in the semiconductor devices, the total harmonic distortion factor and the energy stored by the flying capacitor.

From the comparison resulted the following:

- A lower number of devices and a slightly lower harmonic content at a very low modulation index for the 5L-ANPC-FC converter.
- Better loss distribution, increased maximum output power and a better efficiency regardless of the modulation index for the 5L-AVNPC converter.

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