CMOS DIFFERENTIAL STRUCTURE WITH IMPROVED LINEARITY AND INCREASED FREQUENCY RESPONSE

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Key words: Linearity, Differential structure, CMOS circuits.

An original differential structure using exclusively MOS devices working in the saturation region will be presented. Having the great advantage of an excellent linearity, obtained by a proper biasing of the differential core (using original translation and arithmetical mean blocks), the proposed circuit is designed for low-voltage low-power operation. The simulated linearity is obtained for an extended range of the differential input voltage and in the worst case of considering second-order effects that affect MOS transistors operation. The frequency response of the new differential structure is strongly increased by operating all MOS devices in the saturation region. The circuit is implemented in $0.35\ \mu m$ CMOS technology, SPICE simulations confirming the theoretical estimated results.

1. **INTRODUCTION**

The differential amplifier is an important stage of a very large area of applications, including high-performances analog/mixed ICs, such as operational amplifiers, voltage comparators, voltage regulators, video amplifiers, modulators and demodulators or A/D and D/A converters. The linearity of the classical CMOS differential amplifier is relatively poor because of the fundamental nonlinear characteristic of MOS transistors, resulting the possibility of achieving a relatively good linearity only for a restricted input voltage range (the amplitude of the input voltage for the classic differential amplifier using MOS transistors in saturation have to be below a few hundreds of mV). To conclude, it results the necessity of implementing a linearization technique for decreasing the superior-order nonlinearities of the MOS differential stage and for increasing the input differential voltage range. It exists in literature many circuit techniques used to improve the MOS differential amplifier linearity [1–10]. It was presented in [4, 5] a third and fifth-order harmonics cancellation with good results and a relatively simple circuit implementation. A constant-sum of the gate-source voltages circuit connection was

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described in [6] and it allows an important reduction of the total harmonic distortions coefficient of the circuit. In [7], it was presented and implemented in CMOS technology a simple technique based on square-root circuits for improving the CMOS differential stage linearity, which compensates the quadratic characteristic of the MOS transistor in saturation.

2. **THEORETICAL ANALYSIS**

The original proposed differential amplifier is based on a quasi-symmetrical structure, using exclusively MOS devices operating in the saturation region for improving the circuit frequency response. In order to improve the differential structure linearity, a proper biasing of the differential core will be used, based on original translation and arithmetical mean blocks. As a result of applying original design techniques, the circuit linearity is maintained for an extended range of the differential input voltage, even in the case of considering second-order effects that affect MOS transistors operation.

2.1. THE BLOCK DIAGRAM OF THE LINEARIZED STRUCTURE

The block diagram of the proposed linearized differential structure is presented in Fig. 1. The "DA" block represents a classical current mirror load differential amplifier, having the common-sources point biased at a potential V fixed by the circuit "M". This circuit computes the arithmetical mean of input potentials, assuring a very good linearity of the entire structure, with the contribution of "T" shift level blocks.

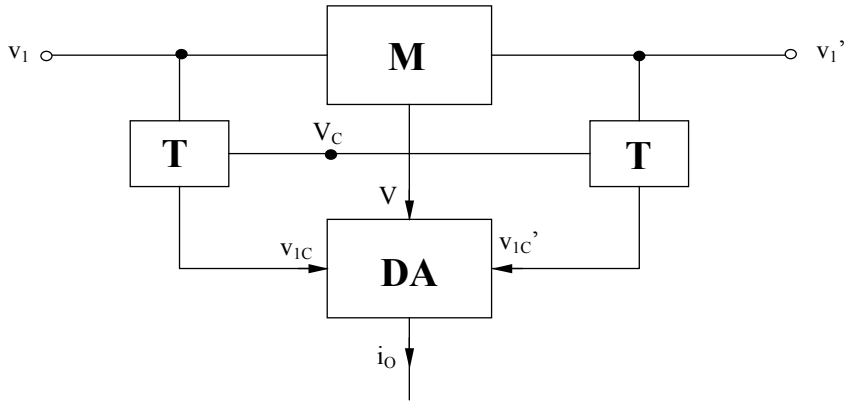

Fig. 1 – The block diagram of the differential structure.

2.2. THE "DA" (DIFFERENTIAL AMPLIFIER) BLOCK

The "DA" block is a current mirror load differential amplifier (Fig. 2).

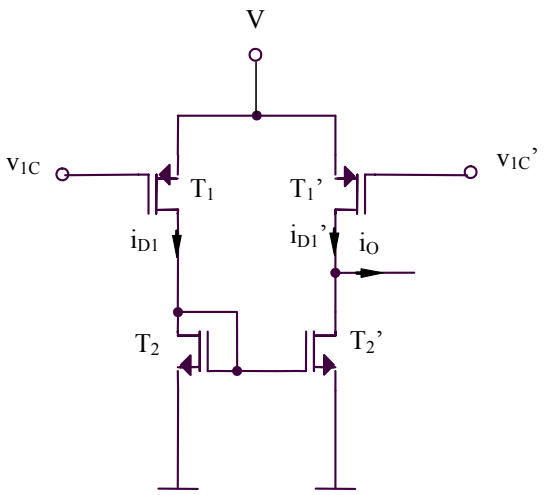

Fig. 2 – The implementation of the "DA" block.

Considering an active region operation of MOS transistors from Fig. 2, the differential amplifier output current, i_0 is:

$$i_0 = i_{D1}' - i_{D1} = \frac{K}{2}\left(v_{SG1}' - V_T\right)^2 - \frac{K}{2}\left(v_{SG1} - V_T\right)^2, \tag{1}$$

equivalent with:

$$i_0 = \frac{K}{2}\left(v_{SG1}' - v_{SG1}\right)\left(v_{SG1}' + v_{SG1} - 2V_T\right). \tag{2}$$

Because:

$$v_{SG} = V - v_{1C} \tag{3}$$

and

$$v_{SG}' = V - v_{1C}', \tag{4}$$

it results

$$i_O = \frac{K}{2}\left(v_{1C} - v_{1C}'\right)\left(2V - v_{1C} - v_{1C}' - 2V_T\right). \tag{5}$$

In order to get a linear transfer characteristic $i_0(v_{1C} - v_{1C}')$, it is necessary that $2V - v_{1C} - v_{1C}' - 2V_T = A$ to be independent on differential input voltage, resulting in:

$$V = \frac{v_{1C} + v_{1C}'}{2} + V_T + \frac{A}{2}. \tag{6}$$

2.3. THE "T" (TRANSLATION) BLOCK

Equation (6) can be implemented by the Fig. 3 circuit.

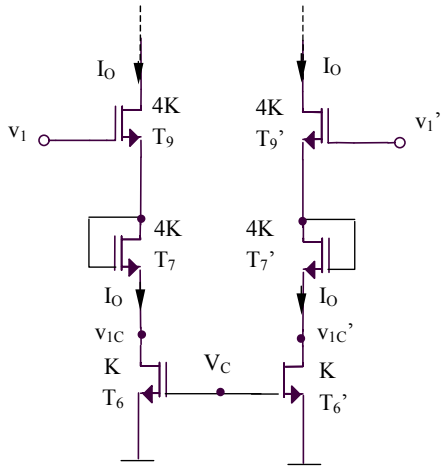

Fig. 3 – The translation block "T".

Because the drain current of all transistors are equal to I_0:

$$I_0 = \frac{4K}{2}\left(\frac{v_1 - v_{1C}}{2} - V_T\right)^2 = \frac{K}{2}\left(V_C - V_T\right)^2, \tag{7}$$

equivalent to

$$v_1 = v_{1C} + V_C + V_T \tag{8}$$

and

$$v_1' = v_{1C}' + V_C + V_T \tag{9}$$

(both input potentials v_1 and v_1' being shifted with the same amount, $V_T + V_C$).

2.4. THE "M" (ARITHMETIC MEAN) BLOCK

In order to get $(v_{ic} + v_{ic}')/2$ term of equation (6) is used Fig. 4 circuit, named "M". This circuit has the advantage of using only MOS transistors biased in saturation region.

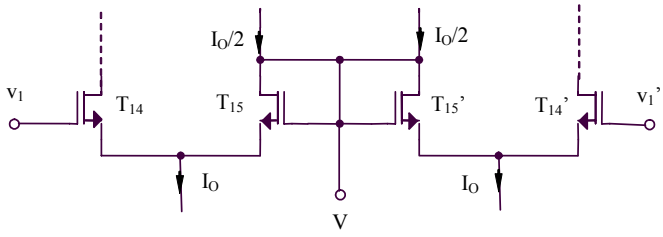

Fig. 4 – The "M" block.

The differential amplifier stages ($T_{14} - T_{15}$ and $T_{14}'–T_{15}'$ transistors) are biased at $I_0/2$ current. As a result, gate-source voltages of T_{14} and T_{15}' transistors are equal and, similarly, gate-source voltages of T_{14}' and T_{15} transistors are equal and:

$$v_1 - V = v_{GS14} - v_{GS15}, \tag{10}$$

$$V - v_1' = v_{GS15}' - v_{GS14}'. \tag{11}$$

From equations (10) and (11) results:

$$V = \frac{v_1 + v_1'}{2} \tag{12}$$

and replacing (8) and (9) in (12), it could be obtained:

$$V = \frac{v_{1C} + v_{1C}'}{2} + V_C + V_T. \tag{13}$$

Comparing equations (6) and (13), it results:

$$A = 2V_C \tag{14}$$

and

$$i_0 = KV_C\left(v_{1C} - v_{1C}'\right), \tag{15}$$

equivalent to (see equations (8) and (9)):

$$i_0 = KV_C\left(v_1 - v_1'\right) = G_m\left(v_1 - v_1'\right). \tag{16}$$

Equation (16) shows a linear dependence of differential amplifier from Fig. 2 output current versus differential input voltage. This linear dependence is a result of new original biasing scheme used. The full implementation of the linearized differential structure is presented in Fig. 5.

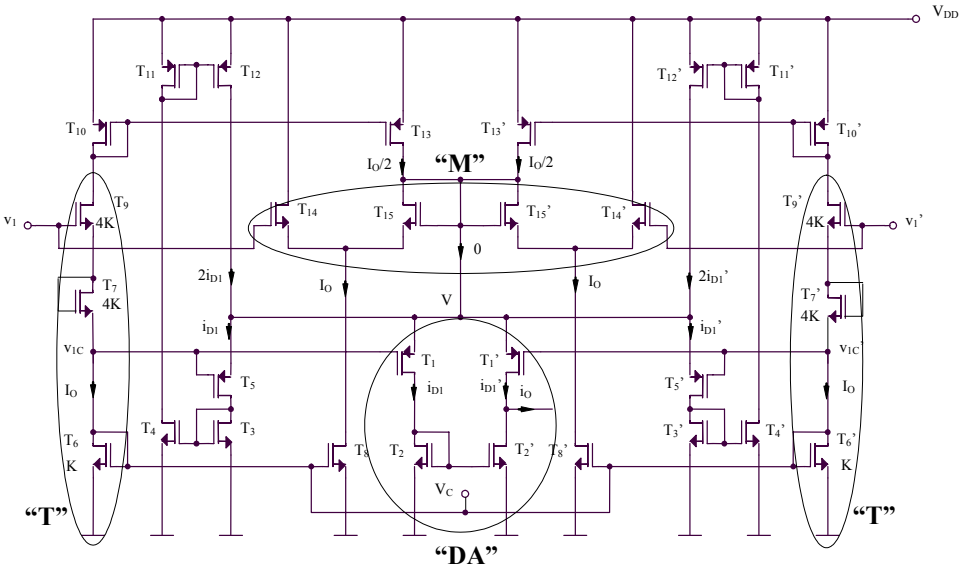

Fig. 5 – The full implementation of the differential structure.

2.5. SECOND-ORDER EFFECTS

The ideal linearity of the proposed differential structure described by equation (16) could be obtained only in a first-order analysis. All of the circuits presented above are affected by the second-order effects like channel length modulation and mobility degradation described by:

$$i_D = \frac{K}{2}\left(v_{SG} - V_T\right)^2\left(1 + \lambda\, v_{SD}\right), \tag{17}$$

$$K = \frac{K_0}{\left[1 + \theta_G\left(v_{SG} - V_T\right)\right]\left(1 + \theta_D v_{SD}\right)}. \tag{18}$$

These second-order effects modify the MOS transistor quadratic law. Considering in this analysis only the errors introduced by the dependence of the carriers' mobility on the gate-source voltage, the drain currents of transistors T_1 and T_1' from Fig. 2 will have the following expressions:

$$i_{D1} = \frac{K}{2}\frac{x^2}{1 + \theta_G x} \tag{19}$$

and

$$i_{D1}' = \frac{K}{2}\frac{x'^2}{1 + \theta_G x'}, \tag{20}$$

where $x \overset{not.}{=} v_{SG1} - V_T$ and $x' \overset{not.}{=} v_{SG1}' - V_T$. In this case, the consideration of second-order effects will conduct to the following expression of the output current of the differential amplifier "DA":

$$i_0 = \frac{K}{2}\left(\frac{x'^2}{1 + \theta_G x'} - \frac{x^2}{1 + \theta_G x}\right). \tag{21}$$

Because $\theta_G x << 1$ and $\theta_G x' << 1$, the previous relation could be approximated as:

$$i_0 \cong \frac{K}{2}\left[\left(x'^2 - x^2\right) - \theta_G\left(x'^3 - x^3\right)\right] \tag{22}$$

Knowing that:

$$x'^3 - x^3 = \left(x' - x\right)\frac{3\left(x' + x\right)^2 + \left(x' - x\right)^2}{4} \tag{23}$$

$$x' - x = v_{SG1}' - v_{SG1} \tag{24}$$

and

$$x' + x = v_{SG1}' + v_{SG1} - 2V_T, \tag{25}$$

it results:

$$i_0 = KV_C\left(v_1 - v_1'\right) + \varepsilon, \tag{26}$$

ε being the error caused by second-order effects:

$$\varepsilon = \frac{K\theta_G}{2}\left(v_{SG1}' - v_{SG1}\right)\frac{3\left(v_{SG1}' + v_{SG1} - 2V_T\right)^2 + \left(v_{SG1}' - v_{SG1}\right)^2}{4}. \tag{27}$$

The difference of gate-source voltages for "DA" circuit is:

$$v_{SG1}' - v_{SG1} = v_{1C} - v_{1C}' = v_1 - v_1', \tag{28}$$

while their sum is:

$$v_{SG1}' + v_{SG1} = 2V - v_{1C} - v_{1C}' = 2V + 2V_C + 2V_T - \left(v_1 + v_1'\right). \tag{29}$$

But $V = \left(v_1 + v_1'\right)/2$, so:

$$v_{SG1}' + v_{SG1} = 2\left(V_C + V_T\right), \tag{30}$$

resulting

$$\varepsilon = \frac{3K\theta_G}{2}V_C^2\left(v_1 - v_1'\right) + \frac{K\theta_G}{8}\left(v_1 - v_1'\right)^3. \tag{31}$$

Because the first term of (31) is linearly dependent on the differential input voltage of the differential amplifier "DA", $v_1 - v_1'$, its presence will be concretize in a very small gain trimming. Thus, the total harmonic distortion coefficient of the circuit could be expressed as the ratio of the second term from (31) – third-order term – and the linear term from (26), resulting:

$$\mathrm{THD}_3 = \frac{\theta_G}{8V_C}\left(v_1 - v_1'\right)^2. \tag{32}$$

For an usual case ($\theta_G = 0.1\mathrm{V}^{-1}$, $V_C = 2\mathrm{V}$ and $v_1 - v_1' = 100\ \mathrm{mV}$), it results $\mathrm{THD}_3 = 6.25\times10^{-5}$. The circuit distortions strongly increases as the amplitude of the input differential voltage increases. It is possible to reduce the value of the total harmonic distortion coefficient even for large values of the input voltage amplitude by using an anti-parallel connection of two differential amplifiers proper designed having different biasing.

3. **SIMULATED RESULTS**

The SPICE simulations $i_0\left(v_1 - v_1'\right)$ based on 0.35 μm CMOS process parameters for the classical and original differential amplifiers are presented in

Fig. 6 and Fig. 7, showing an important improvement of the circuit linearity as a result of applying the original technique. The supply voltage corresponds to low-power requirements, $V_{DD} = 3$ V.

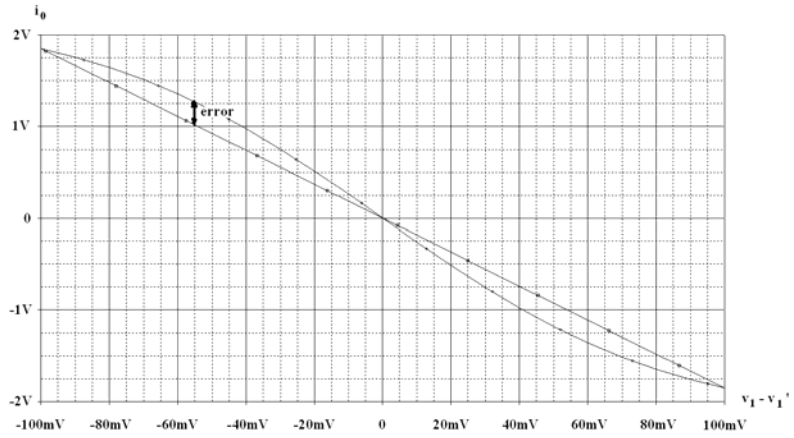

Fig. 6 – Simulations of the transfer characteristic for the classical differential amplifier compared with a perfect linear differential amplifier.

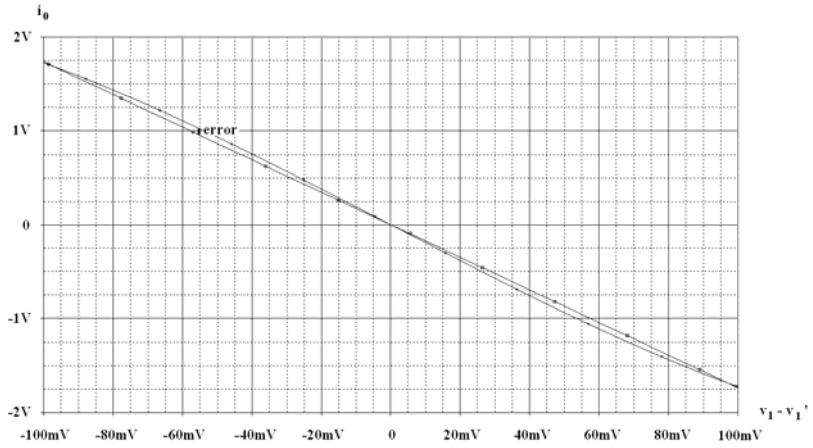

Fig. 7 – Simulations of the transfer characteristic for the linearized differential amplifier compared with a perfect linear differential amplifier.

5. **CONCLUSIONS**

An original differential structure using exclusively MOS devices working in the saturation region has been presented. The proposed circuit offers an excellent

linearity, obtained by a new original biasing of the differential core. The proposed circuit was designed for low-voltage low-power operation. The estimated linearity was obtained for an extended range of the differential input voltage. The second-order effects that affect MOS transistors operation were analysed and their impact has been evaluated. The circuit is implemented in $0.35\mu m$ CMOS technology, the SPICE simulations confirming the theoretical estimated results.

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