

AN IMPROVEMENT OF ULTRA LOW POWER, VOLTAGE AND TEMPERATURE INSENSITIVE CMOS VOLTAGE REFERENCE

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This paper presents the design of a CMOS voltage reference circuit. In the past, the design of a CMOS voltage reference circuit consisted of a lot of active and passive devices or required an external startup circuit. Therefore, this research presents the design of a voltage reference circuit using all CMOS without parasitic bipolar junction transistors (BJT) and passive devices, which cause loss of power and consume a large chip area. It can be operated without external startup circuit. The result of PSPICE (personal simulation program with IC emphasis) simulation program has been verified that the circuit can operate with stability. The supply voltage is only 1.8 V, reference voltage levels of about 259 ± 2.5 mV, the standard temperature coefficient of 95.15 ppm/°C, ranges from -20 to 100 °C and a low power dissipation of 2.93 μ W.

1. INTRODUCTION

Voltage reference circuits have been developed continuously. In particular, CMOS voltage reference circuit presented in the past research is widely used in electronic circuits application such as analog-to-digital and digital-to-analog conversion circuit, oscillators, memory and many more of them [1, 2]. In addition, it can be used with many types of devices such as daily-used portable devices which can be smaller in size with lower consumption [3, 6]. In the past, CMOS voltage reference circuit was developed in many ways such as reducing it to a lower voltage operation [5, 7] and chip area [2, 4] or using the parasitic BJT [8, 12]. These circuits still have some areas to create diode for generating negative and positive current for the temperature coefficient [13].

Therefore, this paper presents all CMOS voltage reference circuit design based on subthreshold voltage without parasitic BJT and external startup circuit by new current summation technique that has opposite coefficient for reference voltage generation which stabilize supply voltage and temperature variations.

2. PRINCIPLE OF A VOLTAGE REFERENCE

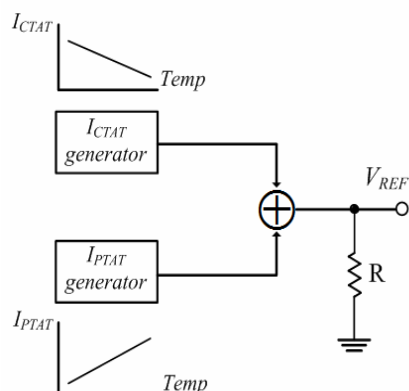


Fig. 1 – Proposed CMOS voltage reference circuit.

The principle of the presented circuit consists of three parts as shown in Fig. 1.

The first part is the current generator circuit with a positive temperature coefficient or proportional to absolute temperature (PTAT). Second part is used for generating the current that has negative temperature coefficient or complementary to absolute temperature (CTAT). Both currents are summed together. The stable voltage (V_{REF}) with a temperature coefficient (TC) can be achieved by this methodology.

3. THE PROPOSED CMOS VOLTAGE REFERENCE

The proposed CMOS voltage reference circuit is shown in Fig. 2.

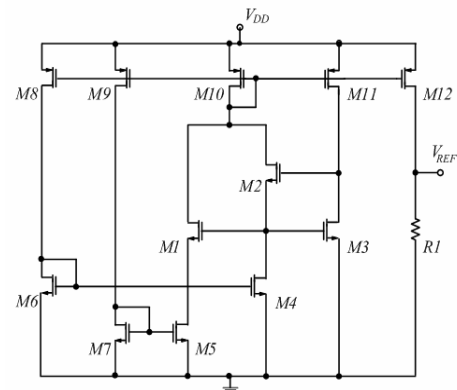


Fig. 2 – Proposed CMOS voltage reference circuit.

The MOS transistors M1 and M3 operated in the subthreshold region is defined as the operating region of the MOS transistor at very low drain currents, with the gate-source voltage V_{GS} values around the threshold voltage V_{th} as adopted by [4]:

$$V_{GS} < V_{th} \quad (1)$$

The V_{GS} of M1 and M3 can be calculated using the current equation in subthreshold regions, as stated below [7]:

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$$V_{GS_{M1}} = nV_T \ln \left(\frac{I_{ds1} \cdot L_1}{I_t \cdot W_1} \right) + V_{th} \quad (2)$$

$$V_{GS_{M3}} = nV_T \ln \left(\frac{I_{ds3} \cdot L_3}{I_t \cdot W_3} \right) + V_{th} \quad (3)$$

where

$$V_T = \frac{kT}{q}, \quad (4)$$

and V_T – is thermal voltage; k – is Boltzmann constant, equal to 1.38×10^{-23} J/°K; q – is electric charges, equal to 1.6×10^{-19} C; T – is test temperature (°K); n – is slope factor in PSPICE, determined to be between 1.5 to 2; I_t – is saturation current of MOS transistor.

The MOS transistors M2, M4, M6 and M7 are defined to operate in the saturation region. The I – V characteristic of a MOS transistor in the saturation region can be well approximated as [5]:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2, \quad (5)$$

where W and L is channel width and channel length of the transistor, C_{ox} is the value of capacitance per unit area of the gate oxide (electron charge per unit area), V_{th} is the threshold voltage and μ_n is the carrier mobility, respectively.

For MOS transistor, the primary parameters that are affected by temperature in equation (5) are the threshold voltage V_{th} and the carrier mobility μ_n . The mobility μ_n depends on the [9]:

$$\mu_n(T) = \mu_n(T_0) \left(\frac{T}{T_0} \right)^{-\beta_\mu}, \quad (6)$$

where $\mu_n(T_0)$ is the mobility of electrons at room temperature, T_0 is room temperature (300° K), T is the test temperature and β_μ is the mobility temperature exponent. The following equation (6) demonstrates the value change of $\mu_n(T)$ at test temperature. That is, when the temperature increases, then $\mu_n(T_0)$ will decrease.

The dependence of the threshold voltage V_{th} to temperature variation is expressed as:

$$V_{th} = V_{th}(T_0) + \alpha_{V_{th}} (T - T_0), \quad (7)$$

where T_0 is the reference temperature, $\alpha_{V_{th}}$ is normally a negative constant. From (7), V_{th} decreases with elevation of the temperature.

The first part is composed of M1, M3, M5 and M7. The V_{GS} in M3 is equal to the sum of V_{GS} in M1 and drain-source voltage V_{DS} in M5 can be written as:

$$V_{GS_{M3}} = V_{GS_{M1}} + V_{DS_{M5}}. \quad (8)$$

From equation (8) we get:

$$V_{DS_{M5}} = V_{GS_{M3}} - V_{GS_{M1}}. \quad (9)$$

Then, the voltage V_{DS} of M5 can be express as:

$$V_{DS_{M5}} = nV_T \ln \left(\frac{I_{ds_{M3}} \cdot W_1 / L_1}{I_{ds_{M1}} \cdot W_3 / L_3} \right). \quad (10)$$

The M5 operating in a linear region uses a modified beta-multiplier self-bias circuit using a MOS resistor, M5, instead of ordinary resistor, as shown in the following equation [9]:

$$R_{M5} = \frac{1}{\mu_n C_{ox} \frac{W_5}{L_5} (V_{GS_{M5}} - V_{th})}. \quad (11)$$

Using equations (10) and (11), we can express I_{PTAT} as:

$$I_{D_{M5}} = I_{PTAT} = \frac{V_{DS_{M5}}}{R_{M5}}, \quad (12)$$

yielding

$$I_{PTAT} = \frac{nV_T}{R_{M5}} \ln \left(\frac{I_{ds_{M3}} \cdot W_1 / L_1}{I_{ds_{M1}} \cdot W_3 / L_3} \right). \quad (13)$$

The study reveals in equation (13), that the current $I_{D_{M5}}$ has a positive temperature coefficient; it's clearly seen that when temperature increases in V_T , the current $I_{D_{M5}}$ will increase.

The second part is composed of M3, M4 and M6. The M3 is defined to operate in the subthreshold region and the V_{GS} of M3 is in equation (3). The gate-source voltage in M6 provides a gate-source voltage for M4 and they are both defined to operate in a saturation region. The following relations find that:

$$V_{GS_{M6}} = V_{GS_{M4}}. \quad (14)$$

The equation for drain current (I_D) of M4 is given by:

$$I_{D_{M4}} = \frac{1}{2} \mu_n C_{ox} \frac{W_4}{L_4} (V_{GS_{M4}} - V_{th})^2. \quad (15)$$

Hence, the drain current has a square-law dependence on the gate-source voltage and the transconductance of M4 is found from differentiating equation (15) with respect to V_{GS} obtained [13]:

$$g_{M4} = \frac{\partial I_{D_{M4}}}{\partial V_{GS_{M4}}} = \frac{1}{2} \mu_n C_{ox} \frac{W_4}{L_4} 2(V_{GS_{M4}} - V_{th}) \quad (16)$$

and we can obtain:

$$g_{M4} = \mu_n C_{ox} \frac{W_4}{L_4} (V_{GS_{M4}} - V_{th}), \quad (17)$$

since

$$R_{M4} = \frac{1}{g_{M4}} = \frac{1}{\mu_n C_{ox} \frac{W_4}{L_4} (V_{GS_{M4}} - V_{th})}. \quad (18)$$

Using equations (3) and (18), we arrive at the expression:

$$I_{D_{M4}} = \frac{V_{GS_{M3}}}{R_{M4}}, \quad (19)$$

yielding

$$I_{D_{M4}} = \frac{nV_T}{R_{M4}} \ln \left(\frac{I_{ds_{M3}}}{I_t} \cdot \frac{L_3}{W_3} \right) + V_{th}. \quad (20)$$

It reveals in equation (20) that $I_{D_{M4}}$ will decrease as temperature increases which is called I_{CTAT} . As shows in equation (19), this implies that the $V_{GS_{M3}}$ is quite small and decreases with the temperature increases [4, 10].

In the last part, the mirror circuit consists of MOS transistor M8 to M12. A reference current (I_{REF}) is the sum of I_{PTAT} and I_{CTAT} by the MOS transistor M10. This can be expressed as:

$$I_{REF} = I_{PTAT} + I_{CTAT}. \quad (21)$$

By using equation (13) and (20), we can express the reference current as:

$$I_{REF} = \frac{nV_T}{R_{M5}} \ln \left(\frac{I_{ds_{M3}}}{I_{ds_{M1}}} \cdot \frac{K_1}{K_3} \right) + \frac{nV_T}{R_{M4}} \ln \left(\frac{I_{ds_{M3}}}{I_t} \cdot \frac{1}{K_3} \right) + V_{th}, \quad (22)$$

where $K_1 = W_1/L_1$ and $K_3 = W_3/L_3$.

The I_{REF} is sourced on a resistor $R1$, thus the reference voltage can be obtained as follows:

$$V_{REF} = I_{REF} R1. \quad (23)$$

The output reference voltage can be adjusted to any level by changing the resistance value of $R1$ and the reference voltage remains stable when the following condition is satisfied [4, 11]:

$$\frac{\partial V_{REF}}{\partial T} = 0. \quad (24)$$

The voltage reference with a TC formed by the min/max limits for the nominal output voltage over the operating temperature range is defined as follows:

$$TC = \frac{1}{V_{atroomtemp}} \left[\frac{V_{max} - V_{min}}{T_{min} - T_{max}} \right] \cdot 10^6 \text{ [ppm/}^\circ\text{C]} \quad (25)$$

The voltage reference circuit exhibits a TC limit typically between 20 to 100 ppm/ $^\circ\text{C}$ [12].

4. SIMULATION RESULTS

The TSMC 0.35 μm of CMOS technology was used to evaluate the performance of the proposed circuit, verified by PSPICE software and a supply voltage $V_{DD} = 1.8$ V. Table 1 shows the parameter size of MOS transistors and resistor.

Table 1

The parameters of transistors and resistors

Transistors	W/L($\mu\text{m}/\mu\text{m}$)
M1	6 / 2.9
M2	6 / 5
M3	8 / 2.3
M4	1.3 / 2.4
M5	2 / 2.4
M6	4.1 / 3.4
M7	2.2 / 1.9
M8 - M11	5 / 5
M12	8 / 5
Aspect ratio M1/M3	2
Resistors	(k Ω)
R1	550

Figure 3 shows the direction when I_{PTAT} and I_{CTAT} were changed, which is associated with the temperature range of -20 to 100 $^\circ\text{C}$.

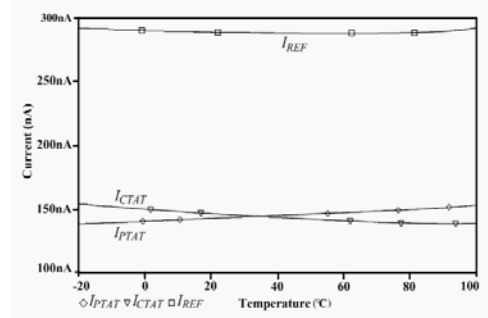


Fig. 3 – The currents I_{CTAT} , I_{PTAT} and I_{REF} as a function of the temperature.

I_{CTAT} will decrease as the temperature increases and I_{PTAT} is increased as the temperature increases. Then the two are combined at MOS transistor M10 to create the current I_{REF} , which is constant and has a low impact on the change in temperature.

Figure 4 shows the output reference voltage as a function at room temperature, that indicates about 259 mV, the voltage variation less than 2.5 mV, the temperature variations of -20 $^\circ\text{C}$ to 100 $^\circ\text{C}$, and the temperature coefficient is 95.15 ppm/ $^\circ\text{C}$.

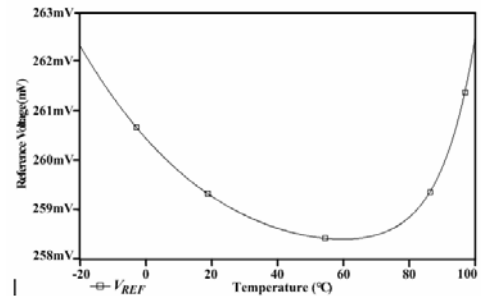


Fig. 4 – Output reference voltage versus temperature.

Simulation result shows that the proposed voltage reference generates a mean reference voltage of about 259

mV with a variation of 1.0 mV/V at room temperature and the power consumption is 2.93 μ W, when the supply voltage increases from 1.8 V to 4.0 V, as shown in Fig. 5.

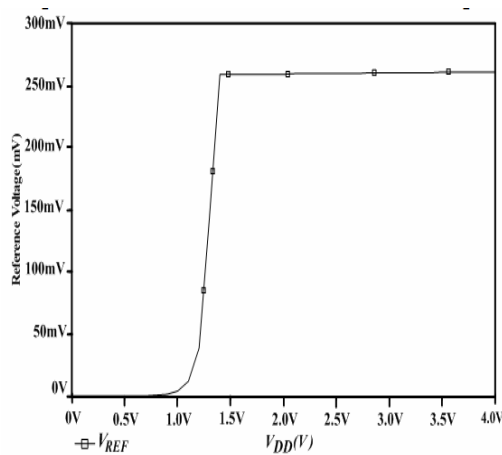


Fig. 5 – Reference voltage as a function of supply voltage.

5. CONCLUSIONS

An all CMOS voltage reference circuit presented in this paper, can work without the external startup circuit, and the work is not complicated because it generates and sums positive and negative currents to a stable voltage reference. This reduces the number of devices that are used as the main components of the circuit. As a result, the circuit consumes lower power. It can be further developed as an integrated circuit. In this circuit, the temperature range is wide (–20 to 100 °C), and stable to supply voltage variation (1.0 mV/V), with a low temperature coefficient of 95.15 ppm/°C, in the TSMC 0.35 μ m CMOS technology, and the output voltage can be adjusted by the output resistor.

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