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AN 8-BIT CURRENT-STEERING DIGITAL TO ANALOG CONVERTER WITH CALIBRATION CAPABILITIES FOR WIRELESS COMMUNICATIONS

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Key words: Calibration methods, Digital to analog converters, (DAC) High speed , Spurious free dynamic range (SFDR), Signal to noise ration (SNR), Signal to noise and distortion ratio (SINAD), Eeffective number of bits (ENOB).

High speed digital to analog converters (DAC) have found extensive use in modern wireless transmission chains before the antenna. An 8-bit current-steering DAC, designed for baseband operation in mobile communication terminals, has been implemented in a 0.18 µm technology node from TSMC. The die active area is 0.23 mm^2. The circuit is low power and consumes 15 mW from 2.5 V analog supply and 5 mW from a digital 1.5 V digital supply. Additionally, we introduce a DAC calibration method which results in a 2-4 dB of SFDR improvement. Simulations that take into account the measurement setup were also performed in order to determine the factors that lead to the parameter degradation, as well as determining other important parameters as SNR, SINAD and ENOB.

1. INTRODUCTION

The performance of a transmitter chain where the output of the DAC is connected to a quadrature mixer is determined by the performance of the analog part and specifically that of the DAC. A common solution is to use a current-steering DAC (Fig. 1), which provides a large resolution range, high speed and an adequate spurious free dynamic range (SFDR) [1]. The parameters of the high speed data converter circuits can be further improved through calibration. Other methods for improving the dynamic parameters could be using a smaller technology node, or increasing the number of bits, or increasing the sampling frequency. While all these solutions provide a visible improvement, the first two will increase the cost of the chip, while the last will augment the power consumed by the circuit.

This paper aims to present the parameters obtained through simulation and measurement for an 8 bit DAC designed in a 0.18 µm mixed signal technology node with 1 poly and 6 metal layers from TSMC.

Our paper is organized as follows: Section 2 presents the design of the 5 + 3 segmented current-steering DAC, Section 3 presents the measurement results for the static parameters: differential nonlinearity (DNL) and integral nonlinearity (INL). In Section 4, a comparison between the obtained measurement results [2] and the simulation results that take into account the measurement conditions, such as the PCB trace parasitic capacitance and inductance, and clock synchronization. Moreover, we present the results for other dynamic parameters such as SNR, SINAD and ENOB and finally, Section 5 contains the conclusions.

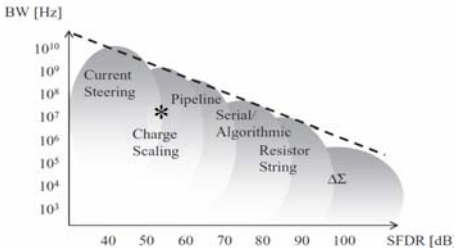

Fig. 1 – DAC architectures in the BW-SFDR plane [1], * our design.

2. CIRCUIT DESCRIPTION

A segmented topology maintains some of the advantages of a thermometric DAC such as low glitches during transitions and an acceptable differential nonlinearity, occupying a low active chip area [3]. For the 8 bit DAC proposed herein, a 5 + 3 segmented architecture was used, where the three least significant bits (LSB) are binary weighted. A thermometer decoder is used in order to activate the 31 unary current cells corresponding to other 5 bits.

In Fig. 2, the schematic of the LSB current cell is presented. The cell consists of a latch connected to an open drain differential pair, which is tailed by a cascade current mirror. A NMOS current mirror was chosen, in order to place devices with higher mobility carriers (with respect to PMOS) in the signal path.

Furthermore, the current of the LSB is set to 40 µA, and the form factor for the LSB current mirror is determined using (1), considering an overdrive voltage of 0.15 V

$$\frac{W}{L} = \frac{I}{K \cdot V_{OV}^2}. \quad (1)$$

From the resulting form factor we obtain the ratio between channel width W and channel length L, and we set $W = 5$ µm, $L = 0.46$ µm, in order to improve the transconductance of the current mirror and the output impedance. Because the transistor occupies a larger area, the resulting (larger) parasitic capacitance will introduce a low frequency pole which will further reduce the bandwidth of the current cell [3].

The MOS switch transistor is designed to use the minimum channel length permitted by the technology and a large channel width of 6 µm to ensure a low on-resistance and parasitic capacitance, while limiting glitches during switching. Transistors M7 and M8 are dummy switches used for charge injection canceling as well as limiting clock feedthrough [4].

The most significant bits are obtained with the thermometric unary cells presented in Fig. 3. Compared to

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the binary-weighted unary cells (Fig. 2), we added two transistors, namely M3, which is used to mirror a fraction of the current, and M2 which is used as a switch for adding the calibration current. With this calibration method we target a minimal total harmonic distortion at the output of the DAC. The calibration method used for the DAC is described in [2, 5–7].

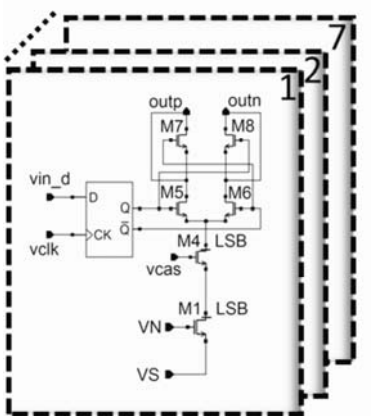

Fig. 2 – Binary weighted current cells.

There are two bias sources, one for the cell current and another one for the calibration current, which can be tuned using of the chip resistors.

An H-tree clock line routing was used to provide an equal delay for all the matrix cells.

In order to maintain symmetry in the output stage, the differential output signal lines were routed in parallel on the third and fourth metal layers. The ground reference line was routed on the top metal layer because of the lower resistivity. During simulations large glitches were observed at the output of the thermometric decoder, so small decoupling capacitors have been added at the 31 outputs.

A serial to parallel interface implemented with 72 latches is used to enable the correction sources.

The active dimensions of the circuit are 0.75 mm x 0.3 mm, while the die size (Fig. 4) is 1.25 mm × 1.25 mm.

The die contains two DACs, the serial to parallel interface with 72 cells, as well as decoupling capacitors that reduce the noise on the digital supply. The digital domain is separated from the analog domain in order to improve the noise characteristic [1]. The IO pads have been provided by TSMC and were chosen to have the smallest capacitance (few hundreds fF) while also providing an adequate electrostatic discharge (ESD) protection.

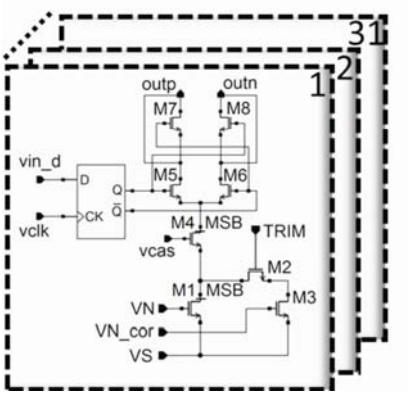

Fig. 3 – Thermometrically coded current cells.

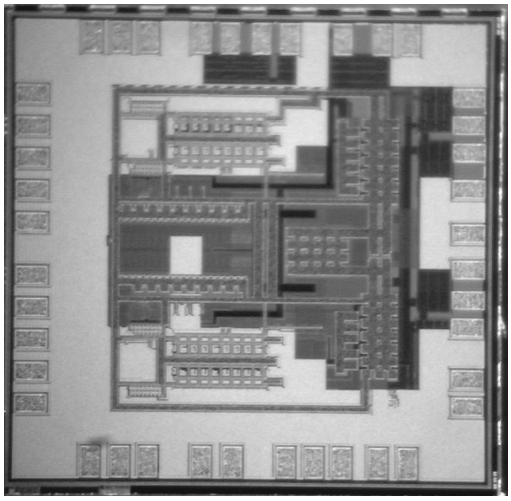

Fig. 4 – Chip die.

3. MEASURMENT RESULTS FOR STATIC PARAMETERS

The DNL is the maximum absolute value of the level difference of two consecutive codes compared to the least significant bit computed from the full scale of the output [1].

The DNL for the input code '*C*' can be written as:

$$\mathrm{DNL}(C) = \frac{\mathrm{Value}(C) - \mathrm{Value}(C-1)}{\mathrm{LSB}}, \tag{2}$$

where

$$\mathrm{LSB} = \frac{\mathrm{Value}(\mathrm{MAX}(C)) - \mathrm{Value}(\min(C))}{\mathrm{MAX}(C) - \min(C)}. \tag{3}$$

The INL is the difference between the output value of the input code and the output value of the same code using an ideal DAC with the same full scale range [1].

The INL for the input code '*C*' can be written as:

$$\mathrm{INL}(C) = \frac{\mathrm{Value}(C) - \mathrm{Value}(0) - C * \mathrm{LSB}}{\mathrm{LSB}} \tag{4}$$

and can be further expressed as a function of the differential nonlinearity:

$$\mathrm{INL}(C) = \sum_{X=0}^{C} \mathrm{DNL}(X). \tag{5}$$

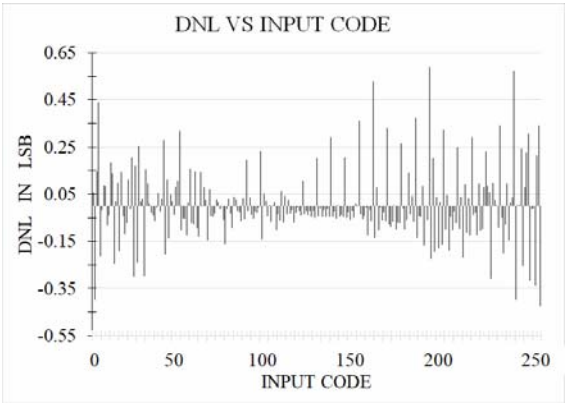

Fig. 5 –Measured DNL for all the input codes.

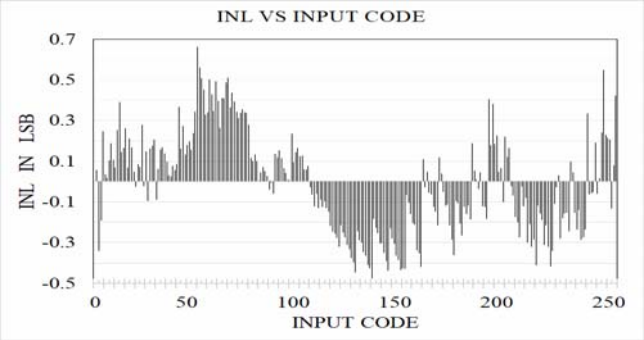

Fig. 6 – Measured INL for all the input codes.

In measurement we obtained approximately 0.6 LSB for DNL (Fig. 5) and 0.7 LSB for INL (Fig. 6). Hence, with respect to the values obtained in simulation, namely 0.268 LSB for INL and 0.377 LSB for DNL, [3], the measured values for the DNL and INL are almost double.

4. SIMULATION OF DINAMIC PARAMETERS

During the measurement of the dynamic parameter SFDR, before and after calibration of the circuit [2], it was observed that at a sampling clock frequency of 500 MHz the results were close to the initial simulation [3], as shown in Table 1. As the sampling frequency of the circuit increased, it was observed that the SFDR, (6), parameter suffered a degradation which was not revealed during simulation. Thus, we performed additional simulations, in order to take into account the effects of the PCB, namely trace capacitance, inductance and resistance, as well as an unsynchronized clock with respect to the input digital signals. Using a clock with a sine waveform and a frequency of 1 GHz, a clock delay between 0 and 900 ps was introduced. In Fig.7, the simulation results for the SFDR parameter when the clock is delayed are presented. The harmonic where the largest spur occurs is also presented. It can be observed that the best result is obtained when the clock is delayed with 0.3 ns and the largest spur occurs at the 5th order harmonic.

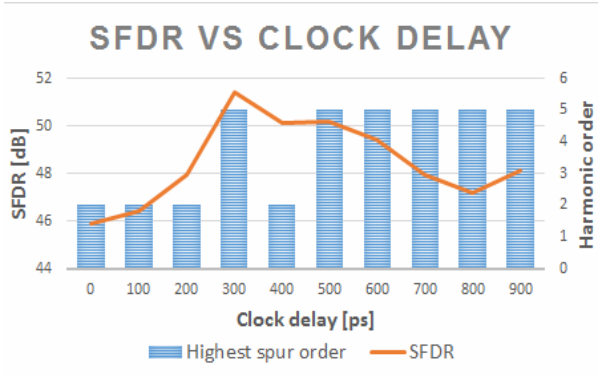

Fig. 7 – SFDR variation with clock delay at nominal technology corner.

Using the transient simulation result for the highest obtained SFDR we determined in Matlab the signal to noise ratio (SNR), (7) and signal to noise and distortion ratio SINAD (Fig. 8). These parameters are calculated with a modified periodogram of the same length as the input signal. The modified periodogram uses a Kaiser window with $\beta = 38$.

Using tone frequencies that are not an integer submultiple of the sampling frequency, as shown in Fig. 9, results in better dynamic performances.

$$\mathrm{SFDR}_{\mathrm{dB}} = 10\log_{10}\frac{P_{sig}}{P_{h\max}} = P_{sig|\mathrm{dBm}} - P_{h\max|\mathrm{dBm}} \tag{6}$$

For both cases the SNR, [1], is calculated after the highest spur is excluded.

The signal to noise and distortion ratio (SINAD or SNDR), (8), is calculated taking into account the noise power as well as the highest spur power.

Table 1

Summary of measurement results before and after calibration at different sampling frequencies

Part #	SFDR in dB					
	5MHz @500Msps		5.5MHz @550Msps		10MHz @1Gsps	
	not cal	cal	not cal	cal	not cal	cal
1	48.7	52	-	-	42.6	45.8
2	48.1	50.1	-	-	41	44
3	-	-	-	-	42.2	44.3
4	-	-	-	-	41.1	42.9
5	-	-	-	-	42.7	45.6
6	49.1	53.2	47.5	49.9	42.1	44.7
7	49.8	53.7	48.3	50.1	-	-
8	48.9	52	47.7	49.9	-	-
9	-	-	47.3	49.8	-	-
10	49.7	53.6	48.8	50.3	-	-
11	-	-	47.9	50	-	-

$$\mathrm{SNR}_{\mathrm{dB}} = 10\log_{10}\frac{P_{sig}}{P_{NOISE}} = P_{sig|\mathrm{dBm}} - P_{\mathrm{NOISE}|\mathrm{dBm}}, \tag{7}$$

$$\mathrm{SINAD}_{\mathrm{dB}} = 10\log_{10}\frac{P_{sig}}{P_{h\max} + P_{\mathrm{NOISE}}}. \tag{8}$$

The effective number of bits (ENOB) is used to determine a maximal obtainable resolution in respect to noise and distortion and can be further calculated using 9:

$$\mathrm{ENOB} = \frac{\mathrm{SINAD} - 1.76}{6.02}. \tag{9}$$

The values obtained are $\mathrm{ENOB}_{10\mathrm{MHz}}$ = 7.53 bits and $\mathrm{ENOB}_{10.172\mathrm{MHz}}$=8.59 bits.

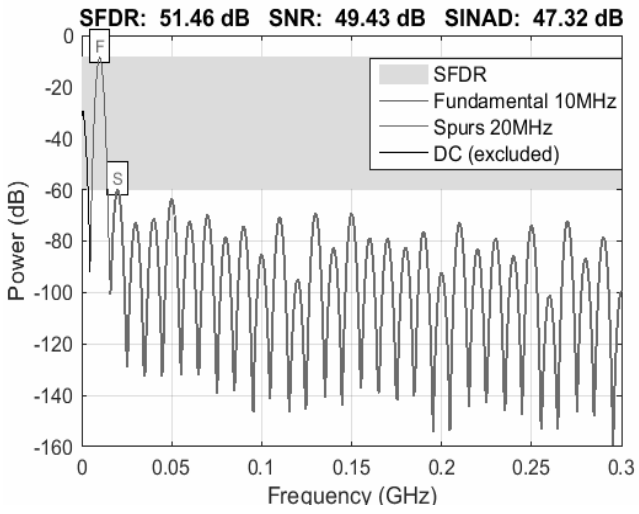

Fig. 8 – Output spectrum for 10 MHz tone.

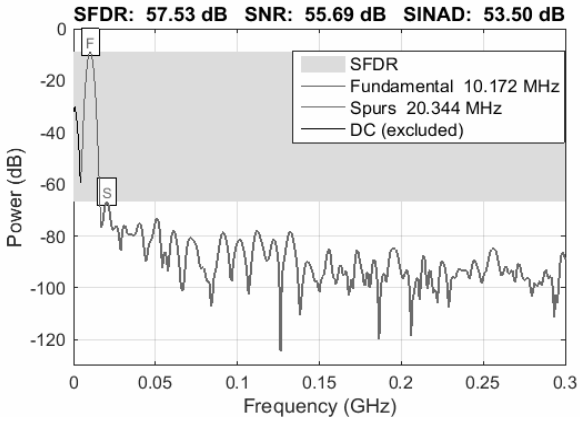

Fig. 9 – Output spectrum for 10.172 MHz tone.

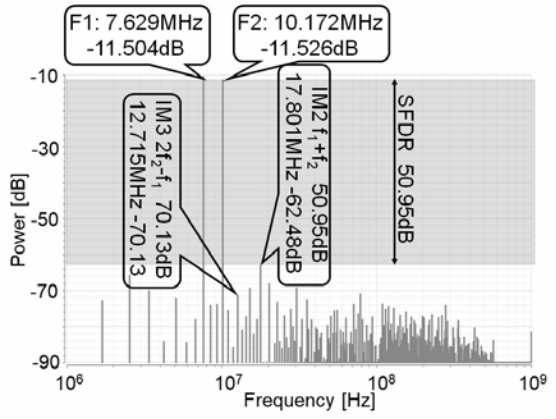

Fig. 10 – Two tone simulation, IM2 and IM3 points are marked.

Distortion due to nonlinearity, [1], also referred as intermodulation distortion (IMD), introduces a number of additional tones at frequencies $k_1 \cdot f_1 + k_2 \cdot f_2$, with k_1 and k_2 arbitrary integer values. These tones, IM_n, are called intermodulation products of order $n = |k_1| + |k_2|$. We can determine the IM2 and IM3 points when performing a two-tone simulation at a frequency of 7.629 MHz and a frequency of 10.172 MHz (Fig. 10). The highest second intermodulation point, IM2, is at the f_1+f_2 frequency and is also the SFDR, while the highest third intermodulation IM3 point is at $2f_2–f_1$.

In Table 2 [2], a comparison with other works in the same or a close technology node is presented. A figure of merit that takes into account the specified parameters is proposed:

$$\mathrm{FOM} = \frac{\mathrm{SFDR} \cdot \mathrm{Process} \times \mathrm{Bandwidth} \times \mathrm{Sample\ rate}}{100 \cdot \mathrm{Resolution} \times \mathrm{Area} \times \mathrm{Power}}. \quad (10)$$

5. **CONCLUSIONS**

An 8 bit DAC was designed and manufactured in TSMC 0.18µm technology. The SFDR obtained in simulation after parasitic extraction is above 50 dB for the 10 MHz bandwidth. After measurement before and after calibration the SFDR remained over 50 dB only for the 500 MHz clock. The measured DNL/INL are approximatively 0.6/0.7 LSB. We have shown that in the case of a two-tone simulation, the SFDR remains above the 50 dB value. After calibration, the DAC in this paper obtained the best figure of merit among the works presented.

Table 2

Comparison with other worksParameter	This work	[8]	[9]	[10]
Technology (µm)	0.18	0.18	0.13	0.13
Resolution (Bits)	8	14	8	8
Sample rate (MSPS)	500	100	700	650
SFDR (dB)	52.4	46.6	53	56
Bandwidth (MHz)	5	30	1	3
Power(mW)	25	79.2	10	18
Area(mm^2)	0.23	0.74	0.5*	0.6
(FOM)	5.13	0.3	1.21	1.64

* estimated value

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