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LINEARLY TUNABLE VOLTAGE DIFFERENCING BUFFERED AMPLIFIER

WORAPONG TANGSRIRAT

Key words: Voltage differencing buffered amplifier (VDBA), Current squarer, MOS analog circuits, Electronically tunable circuit, All-pass filter.

This paper proposes an alternative circuit technique for the implementation of the CMOS-based voltage differencing buffered amplifier (VDBA) with linearly tunable transconductance gain. The realization scheme is based on employing the current-mode squaring function circuit and a pair of active loaded differential-input amplifiers. The current squarer acts as the long-tail biasing current for the differential-input amplifier, achieving its linear tunability. Accordingly, the transconductance gain of the proposed CMOS VDBA is variable linearly and electronically through the external dc bias current. In addition to improve the linear input voltage range, the source degeneration technique is performed. An application of the proposed VDBA as an active tunable first-order all-pass filter has also been described. Simulation results performed using PSPICE program with TSMC 0.25 µm real CMOS technology evaluate the circuit performance and workability.

1. INTRODUCTION

In recent decades, the tremendous growth for the state-of-the-art analog circuit design using different modern active building blocks provide solution to several analog circuit and system challenges. Meanwhile in the recent work [1], various types of novel analog active circuit elements and their small-signal models have also been reviewed and summarized. Among these, the voltage differencing buffered amplifier (VDBA) is a relatively new reported active element, which has simple structure and electronic controllability in a wide range. Numerous applications based on the use of VDBAs as active components have been proposed in the available literature [2–10]. Owing to the fact that the VDBA is a cascade connection of an operational transconductance amplifier as an input stage and a voltage buffer as an output stage, it can operate in both voltage and current mode, which has proved to be functionally flexible and versatile active circuit component. Moreover, the important feature of the VDBA is in built electronic control property of its transconductance gain (g_m), which can be utilized for adjusting the various circuit parameters. In [4–9], some VDBA architectures in CMOS technology have been reported. However, all of them cannot perform linear adjustability of their transconductance gains. In practice, it seems to be more useful and advantage if the CMOS VDBA can provide linearly tunable transconductance gain instead of non-linear tunable ones.

In this work, a CMOS integrable circuit design for the realization of the linearly tunable VDBA with wide-input dynamic range is presented. To achieve the linear transconductance adjustability, the CMOS current squaring circuit is employed for providing the bias current source of the proposed VDBA, where all the transistors are biased in saturation region. Additionally, the source degeneration technique is adopted to improve the input voltage dynamic range, and enhance input resistance level of the designed VDBA. The improvement of circuit performance has been discussed and evaluated with PSPICE simulation results using 0.25 µm TSMC real CMOS process parameters. Finally, an application example in realizing an electronically tunable first-order all-pass filter is designed and simulated to demonstrate the feasibility of the proposed VDBA circuit.

2. BASIC PRINCIPLE OF THE VDBA

The VDBA is a recently introduced four-terminal versatile active building block, as symbolically shown in Fig.1(a). According to the equivalent model of Fig.1(b), this device has four terminals , *i.e.* p, n, z and w, which ideally possesses high-impedance voltage inputs at p and n terminals, high-impedance current output at z terminal and low-impedance voltage output at w terminal. The voltage-current characteristic of the VDBA can be defined by the following expression:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_w \end{bmatrix} . \qquad (1)$$

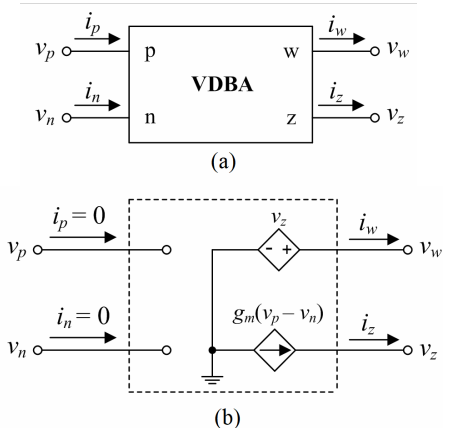

Fig. 1 – The VDBA
(a) circuit diagrammatic representation (b) equivalent circuit.

In above relation (1), the small-signal transconductance gain denoted as g_m is generally adjusted by external dc bias current. Also note from (1) that the differential input voltage between p and n terminals ($v_{id} = v_p - v_n$) is

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converted to a current following out of z terminal (i_z) by g_m. At the same time, the voltage potential at z terminal (v_z) is then copied to w terminal (v_w) with unity-gain amplification or $v_w = v_z$.

3. CMOS CURRENT-SQUARING CIRCUIT

3.1 PRINCIPLE OF OPERATION

The CMOS current-mode squaring functional circuit based on a dual translinear loop M_{1B}-M_{4B} is shown in Fig.2. We will utilize this circuit as a biasing current circuit for the proposed VDBA. All the transistors are assumed to be matched and operated in saturation mode. Using the square-law *I-V* relation, the drain-to-source current (I_{DS}) of the saturated transistor is assumed:

$$I_{DS} = K\left(V_{GS} - V_{TH}\right)^2 \quad , \tag{2}$$

with $K = \frac{\mu C_{ox}}{2}\frac{W}{L}$ as the transconductance parameter, μ as an average channel carrier mobility, C_{ox} as the gate-oxide capacitance per unit area, W and L as the channel width and length of the transistor, respectively, V_{GS} as the gate-to-source voltage, and V_{TH} as the threshold voltage.

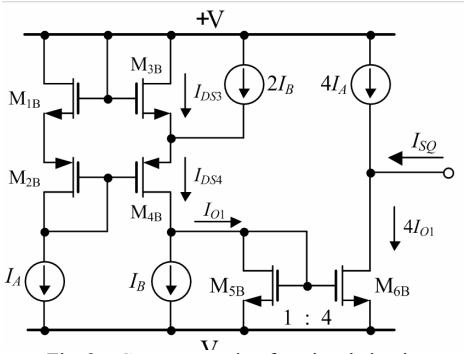

Fig. 2 – Current squaring functional circuit.

Applying Kirchhoff voltage law (KVL) in the dual translinear loop, it is obtained below:

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4}\,. \tag{3}$$

According to (2), and assuming equal transconductance parameters and $I_A = I_{DS1} = I_{DS2}$, Eq.(3) modifies to :

$$\sqrt{I_{DS1}} + \sqrt{I_{DS2}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} = 2\sqrt{I_A} \quad . \tag{4}$$

From Fig.2, the relation of current I_{DS4} of M_{4B} can be expressed as:

$$I_{DS3} = I_{O1} - I_B \quad \text{and} \quad I_{DS4} = I_{O1} + I_B. \tag{5}$$

Replacing (5) in (4) and squaring both sides results in

$$\left(I_{O1} - I_B\right) + \left(I_{O1} + I_B\right) + 2\sqrt{I_{O1}^2 - I_B^2} = 4I_A \quad . \tag{6}$$

Squaring both sides again, we have the following current relation:

$$4I_{O1}^2 - 16I_{O1}I_A + 16I_A^2 = 4\left(I_{O1}^2 - I_B^2\right) \quad . \tag{7}$$

After mathematical manipulations, we obtain the current I_{O1} of Fig. 2 as:

$$I_{O1} = \frac{I_B^2}{4I_A} + I_A\,. \tag{8}$$

The current I_{O1} is then copied to the output node by means of a current mirror M_{5B}-M_{6B} with a 1 : 4 current ratio, resulting in $I_{SQ} = 4(I_{O1} - I_A)$. Therefore, the output current I_{SQ} of Fig. 2 is now:

$$I_{SQ} = \frac{I_B^2}{I_A} \quad . \tag{9}$$

Above equation clearly indicates that the output current I_{SQ} gives squaring function of the input current I_B, divided by I_A. Accordingly, the circuit works as a current squaring functional circuit. In the following section, the CMOS VDBA with linearly tunable transconductance will then be described by utilizing the circuit of Fig.2 as a current biasing circuit.

3.2 SECOND-ORDER EFFECTS

In practice, the various second-order effects of the devices such as body effect and transistor mismatch will degrade the performance of the circuit. In this section, the influence of these non-idealities will be investigated separately.

3.2.1 BODY EFFECTS

It is in general known that the threshold voltage V_{TH} of the MOS transistor is directly dependent on the source-to-bulk voltage (V_{SB}). This effect is the so-called "body effect", which can most conveniently expressed as change in V_{TH} [11],

$$V_{TH} = V_{TH0} + \gamma\left[\sqrt{\left|2\varphi_b + V_{SB}\right|} - \sqrt{2\varphi_b}\right] \quad . \tag{10}$$

In (10), V_{TH0} is the zero-bias threshold voltage, γ is the body-effect constant, and φ_b is the substrate potential. Consider the dual translinear loop M_{1B}-M_{4B} in Fig. 2. The substrates of transistors M_{1B} and M_{3B} are connected to the source, resulting in $V_{SB} = 0$ and $V_{TH} = V_{TH0}$, but this is not in M_{2B} and M_{4B} or $V_{SB} \neq 0$. On considering the mismatch between M_{2B} and M_{4B}, one can assume that:

$$V_{TH2} = V_{TH} + \delta \quad \text{and} \quad V_{TH4} = V_{TH} - \delta \quad , \tag{11}$$

where $\delta << V_{TH}$ is the small deviation between V_{TH2} and V_{TH4}. As a result, this kind of mismatch changes I_{O1} to I'_{O1}.

Substituting (11) into (3) and let $I_A = I_{DS1} = I_{DS2}$, $I_{DS3} = I'_{O1} - I_B$, $I_{DS4} = I'_{O1} + I_B$ and $V_{TH1} = V_{TH4}$ ($|V_{SB}| = 0$), it results:

$$\sqrt{\frac{I'_{O1} + I_B}{K}} + \sqrt{\frac{I'_{O1} - I_B}{K}} = 2\sqrt{\frac{I_A}{K}} + 2\delta\,. \tag{12}$$

Taking the mathematical manipulations by squaring both sides and ignoring δ^2 terms, the current is I'_{O1} then

$$I'_{O1} = \frac{I_B^2}{4I_A\left(1 + 2\delta\sqrt{\frac{K}{I_A}}\right)} + I_A\left(\frac{1 + 4\delta\sqrt{\frac{K}{I_A}}}{1 + 2\delta\sqrt{\frac{K}{I_A}}}\right). \tag{13}$$

Since $I'_{SQ} = 4I'_{O1} - 4I_A$, the output current I'_{SQ} due to body effect is found as:

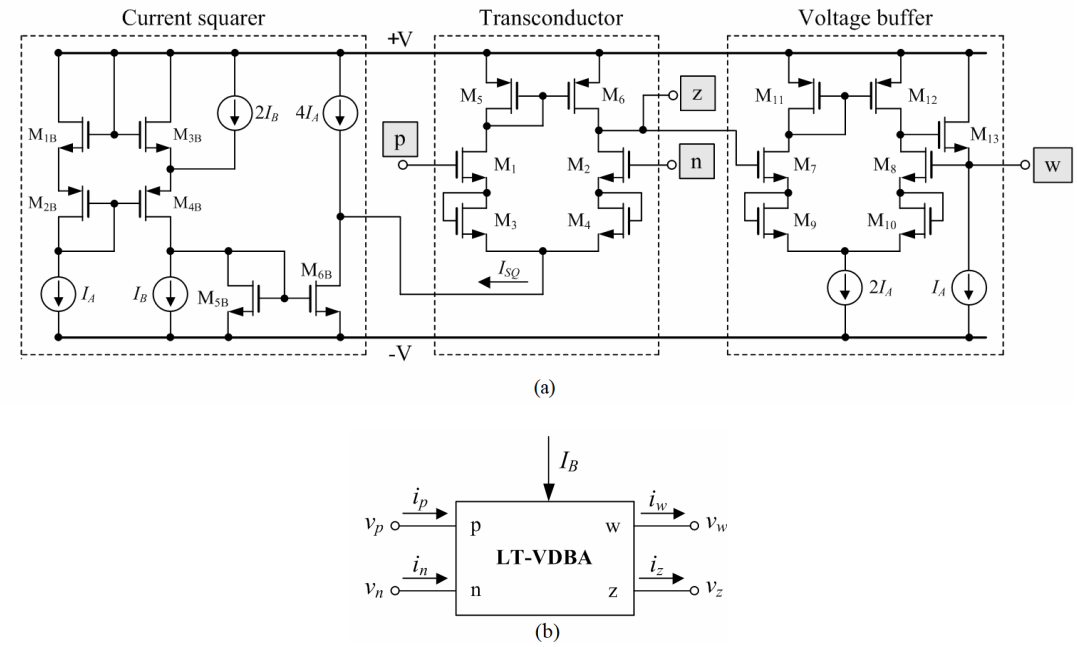

Fig. 3 – Proposed linearly tunable VDBA (LT-VDBA)
(a) complete schematic (b) its associated symbol.

$$I'_{SQ} = \frac{I_B^2}{I_A\left(1+2\delta\sqrt{\frac{K}{I_A}}\right)} + \frac{8\delta\sqrt{KI_A}}{\left(1+2\delta\sqrt{\frac{K}{I_A}}\right)}. \quad (14)$$

Subtracting (9) from (14) results in

$$\Delta I_{SQ} = I_{SQ} - I'_{SQ}.$$

$$= \frac{I_B^2}{I_A} - \frac{I_B^2}{I_A\left(1+2\delta\sqrt{\frac{K}{I_A}}\right)} - \frac{8\delta\sqrt{KI_A}}{\left(1+2\delta\sqrt{\frac{K}{I_A}}\right)}. \quad (15)$$

If $1 >> 2\delta\sqrt{\frac{K}{I_A}}$, then the absolute current deviation from that given by (9) is obtained as:

$$\left|\Delta I_{SQ}\right| \cong 8\delta\sqrt{KI_A}. \quad (16)$$

3.2.2 TRANSISTOR MISMATCH

If the transconductance parameters of NMOS and PMOS devices are mismatched ($K_N \neq K_P$), assume that $K_N = K + \Delta k$, $K_P = K - \Delta k$ and $K >> \Delta k$, Eq.(4) can be re-written as:

$$\sqrt{\frac{I_A}{K_N}} + \sqrt{\frac{I_A}{K_P}} = \sqrt{\frac{I'_{O1} - I_B}{K_N}} + \sqrt{\frac{I'_{O1} + I_B}{K_P}}. \quad (17)$$

Solving (17) for I'_{O1} with ignoring the terms containing $(\Delta k)^2$, it is straightforward to represent that

$$I'_{O1} = \frac{I_B^2}{4I_A\left[1+\left(\frac{I_B}{2I_A}\right)\left(\frac{\Delta k}{K}\right)\right]} + I_A\left[\frac{1+\left(\frac{I_B}{I_A}\right)\left(\frac{\Delta k}{K}\right)}{1+\left(\frac{I_B}{2I_A}\right)\left(\frac{\Delta k}{K}\right)}\right] \quad (18)$$

with $I'_{SQ} = 4I'_{O1} - 4I_A$, the output current I'_{SQ} due to transistor mismatch is thus expressed by:

$$I'_{SQ} = \left[\frac{I_B^2}{4I_A} + 2I_B\left(\frac{\Delta k}{K}\right)\right]\left[\frac{1}{1+\left(\frac{I_B}{2I_A}\right)\left(\frac{\Delta k}{K}\right)}\right]. \quad (19)$$

Since $\Delta I_{SQ} = I_{SQ} - I'_{SQ}$, and assume that $1 >> \left(\frac{I_B}{2I_A}\right)\left(\frac{\Delta k}{K}\right)$, the absolute error can be approximated as:

$$\left|\Delta I_{SQ}\right| \cong 2I_B\left(\frac{\Delta k}{K}\right). \quad (20)$$

4. PROPOSED LINEARLY TUNABLE VDBA

The complete CMOS structure of the proposed linearly tunable VDBA (LT-VDBA) is shown in Fig.3(a), while the corresponding notation is given in Fig.3(b). The proposed circuit is based on the current squaring circuit M_{1B}-M_{6B} of Fig.2, active loaded differential amplifier M_1-M_6 and a voltage buffer M_7-M_{13}. In order to achieve the linear transconductance tunability, the current squarer circuit in Fig.2 creates the bias current I_{SQ} for the circuit. Transistors M_5-M_6 and M_{11}-M_{12} construct the active load, while transistors M_3-M_4 and M_9-M_{10} serve as resistance simulators to enhance the input dynamic range of the circuit. Note that in Fig.3(a), an additional transistor M_{13} forms the negative feedback path from node w to the drain terminal of M_8, in order to provide an exact voltage following with low-output resistance at w terminal [12].

Consider the circuit of Fig. 3. The transconductance gain (g_m) of the proposed LT-VDBA, which is directly scaled by I_{SQ}, can be written as: [8, 9]

$$g_m = \sqrt{2KI_{SQ}} \quad . \tag{21}$$

Replacing I_{SQ} from (7), we obtain the expression for g_m as:

$$g_m = K_m I_B \quad , \tag{22}$$

where $K_m = (2K/I_A)^{1/2}$ and stands for a constant value. Since transconductance change in (12) is provided directly with I_B current, the proposed LT-VDBA circuit of Fig.3 has the linearly electronic tuning feature. Small-signal parasitic resistances at terminals p, n, z and w of the proposed LT-VDBA in Fig.3 are respectively expressed as :

$$R_p = R_n \cong \infty \quad , \tag{23}$$

$$R_z \cong \left(\frac{1}{g_{d2} + g_{d6}} \right) \tag{24}$$

and

$$R_w \cong \left[\frac{(g_{m7} + g_{m8})(g_{d8} + g_{d10})}{g_{m7} g_{m8} g_{m11}} \right] \quad , \tag{25}$$

where g_{mi} and g_{di} are transconductance and drain conductance of related transistor, respectively.

5. SIMULATION RESULTS AND DISCUSSIONS

Results of simulations on the proposed LT-VDBA in Fig.3 are presented in this section. In simulation purpose, PSPICE program using 0.25 μm TSMC CMOS technology is performed with transistor aspects given in Table I. The circuit is designed for supply voltages of +V = –V = 0.75 V and bias currents of I_A = 50 μA.

Table 1

Transistor aspect ratios (*W*/*L*) in the proposed LT-VDBA of Fig.3.

Transistors	*W*/*L* (μm/(μm)
M_1-M_2 , M_7-M_8 , M_{13}	40/0.25
M_3-M_4 , M_9-M_{10}	52/0.25
M_5, M_{11}	32/0.25
M_6, M_{12}	35/0.25
M_{1B}, M_{3B}	9/0.25
M_{2B}, M_{4B}	6/0.25
M_{15B}	15/0.25
M_{16B}	44/0.25

Figure 4 shows variation of the VDBA's transconductance (g_m) with respect to the bias current I_B, compared with the calculated curve. As noted earlier, the variation in I_B directly controls the value of g_m, which makes the proposed LT-VDBA linearly and electronically tunable. It becomes apparent that the g_m value can linearly tune by the bias current I_B over the current range of 0 μA to 260 μA, where the linearity error is less than 4.6 %. Also in Fig.5, the simulated dc transfer characteristic curves between v_{id} (here $v_{id} = v_p - v_n$) and i_z for I_B = 150 μA are plotted, in which its linearity input region of about ±100 mV is observed. Compared to conventional VDBA in [8, 9], as shown in Fig.5, the proposed circuit exhibits wider input voltage range. The circuit dissipates power of approximately 1.37 mW.

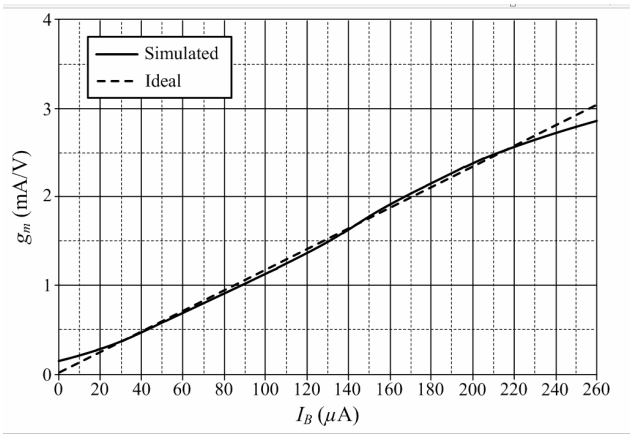

Fig. 4 – Transconductance characteristics of the proposed LT-VDBA in Fig.3.

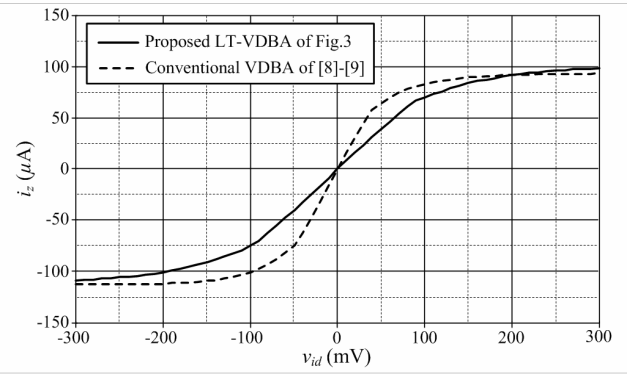

Fig. 5 – Simulated dc transfer characteristics between v_{id} and i_z.

The simulated dc and ac transfer characteristics between v_{id} and i_z of the proposed LT-VDBA according to the changing the bias current I_B are also given in Figs.6 and 7, respectively. As can be seen from these graphs, for the I_B value is changed from 100 μA, 150 μA to 200 μA, the g_m value can be altered electronically from 1.30 mA/V, 1.95 mA/V to 2.40 mA/V, respectively. The simulated frequency response of the voltage gain v_w/v_z of the proposed LT-VDBA is given in Fig.8. It is clear that the voltage gain of v_w/v_z is found to be 0.991, and the voltage transfer bandwidth is about 200 MHz for the maximally flat gain.

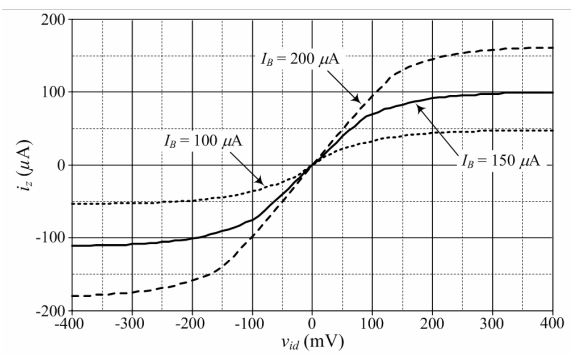

Fig. 6 – Simulated dc transfer characteristics between v_{id} and i_z of the proposed LT-VDBA with tuning I_B.

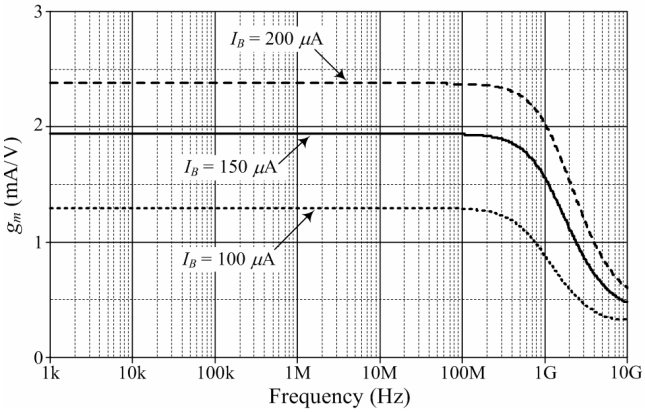

Fig. 7 – Simulated ac transfer characteristics of g_m with tuning I_B.

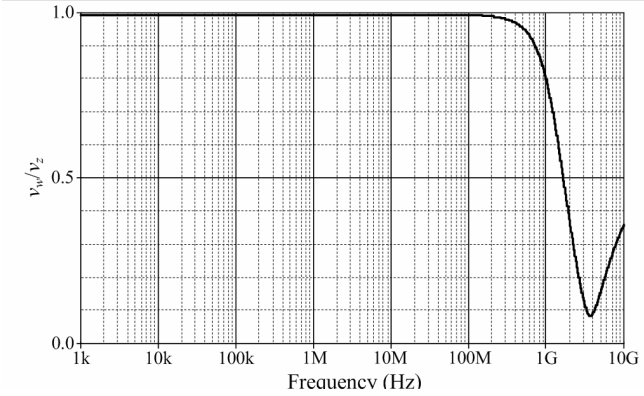

Fig. 8 – Simulated ac transfer characteristics between v_w and v_z (v_w/v_z) of the proposed LT-VDBA.

The simulated frequency characteristics of the parasitic resistance magnitudes on input terminals are given in Fig.9. It is observed that equivalent resistance values are obtained as: $r_p \cong 270$ MΩ and $r_n \cong 110$ MΩ at 100 kHz for p and n terminals, respectively. The simulation results for the parasitic resistance magnitudes on output terminals are also provided in Figs.10 and 11. They are equal to $r_z \cong 445$ kΩ for frequencies below 3 MHz and $r_w \cong 46$ Ω for frequencies below 300 MHz. Comparison between the proposed LT-VDBA in Fig.3 and the four previously reported CMOS VDBAs is included in Table 2.

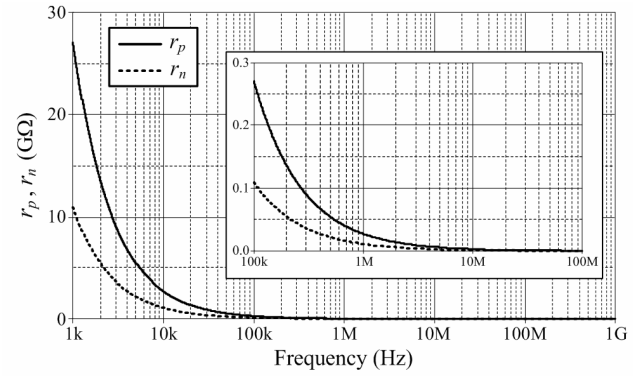

Fig. 9 – Magnitude frequency responses of the parasitic resistances at p and n-terminals (r_z and r_n)

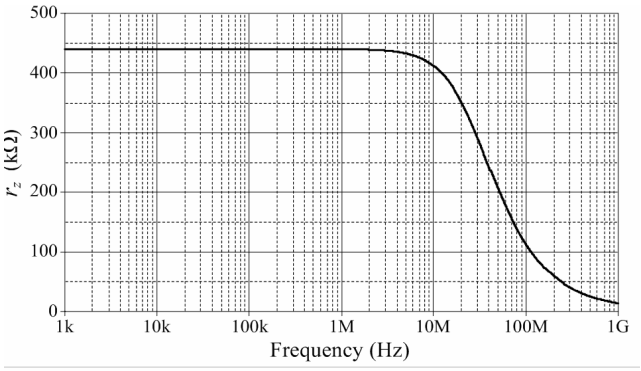

Fig. 10 – Magnitude frequency response of the parasitic resistance at z-terminal (r_z).

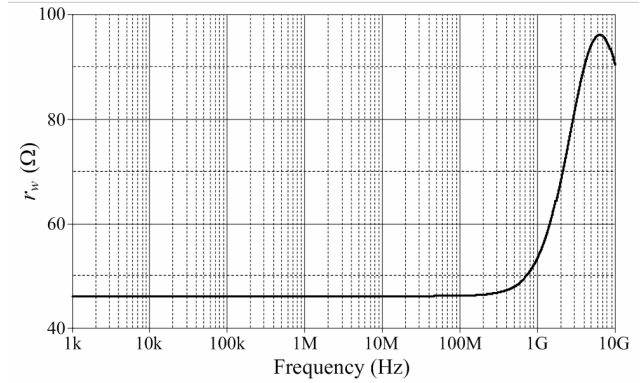

Fig. 11 – Magnitude frequency response of the parasitic resistance at w-terminal (r_w).

Table 2

Performance comparison of the proposed LT-VDBA with the previously reported ones.

Parameter	Proposed LT-VDBA	[4]	[5]	[6]	[8], [9]
CMOS technology	0.25 µm TSMC	0.18 µm TSMC	0.35 µm TSMC	0.18 µm TSMC	0.25 µm TSMC
Supply voltages	±0.75 V	±1.2 V	±1.5 V	±0.2V	±0.75 V
Power dissipation	1.37 mW	Not reported	0.97 mW	6.22 nW	0.3 mW
g_m	0.62 mA/V (@I_B = 50 µA)	0.5 mA/V (@I_B = 50 µA)	0.75 mA/V	64 nA/V	0.26 mA/V (@I_B = 50 µA)
Parasitic resistance at p-terminal	270 MΩ (@ 100 kHz)	Not reported	Not reported	877 GΩ	1.45 GΩ
Parasitic resistance at n-terminal	110 MΩ (@ 100 kHz)	Not reported	Not reported	500 GΩ	1.78 GΩ
Parasitic resistance at z-terminal	445 kΩ	170 kΩ	315 kΩ	5.26 MΩ	276 kΩ
Parasitic resistance at w-terminal	46 Ω	53 Ω	21 Ω	205 Ω	26 Ω
Differential-input voltage range	±100 mV	±75 mV	±200 mV	±50 mV	±50 mV
Bandwidth	200 MHz	160 MHz	Not reported	3.66 kHz	52 MHz

6. ACTIVE VOLTAGE-MODE FIRST-ORDER ALL-PASS FILTER REALIZATION

To establish the applicability of the proposed LT-VDBA in Fig.3, the first-order all-pass filter or the phase-shifter circuit is realized. Basing on one VDBA, the tunable all-pass filter which consists of only one floating capacitor and

one grounded resistor is constructed, and is shown in Fig.12. It should be noted that a floating capacitor is required in the filter realization. However, it can be fabricated easily as a double poly (poly1–poly2) capacitor in advanced integrated circuit design [13]. Routine circuit analysis of the filter in Fig. 12 using relation (1) yields the following voltage transfer function as :

$$\frac{V_o(s)}{V_{in}(s)} = g_m R \left(\frac{\frac{sC}{g_m} - 1}{sRC + 1} \right) \tag{26}$$

If $g_m = 1/R$, the phase characteristic of the circuit has the following form;

$$\phi = \pi - 2\tan^{-1}\left(\frac{\omega C}{g_m}\right) , \tag{27}$$

and the pole frequency is obtained as :

$$\omega_o = 2\pi f_o = \frac{g_m}{C} . \tag{28}$$

From the above, it is readily obtained that the circuit of Fig.12 works as an inverting-type all-pass filter with low-output impedance. Consequently, it can be considered as a cascadable voltage-mode circuit.

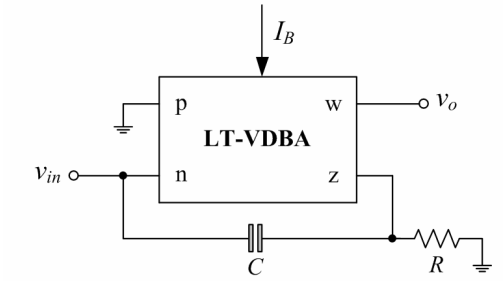

Fig. 12 – Active tunable voltage-mode first-order all-pass filter realization using the proposed LT-VDBA.

The critical sensitivities of the ω_o with respect to active and passive circuit components for the filter are found to be:

$$S_{g_m}^{\omega_o} = -S_C^{\omega_o} = 1 . \tag{29}$$

As a design example to realize the all-pass filter in Fig.12 with the pole frequency of f_o = 1.06 MHz, the circuit is built with I_B = 54 μA ($g_m \cong$ 670 μA/V), R = 1.5 kΩ and C = 100 pF. To investigate the voltage swing capability and the phase error of the circuit, the transient response analysis is performed by stimulating the filter in Fig.12 with a 1.06 MHz frequency sinusoidal voltage signal. The simulated v_{in} and v_o waveforms comparing with the ideal curves are shown in Fig.13. From simulation results, the maximum power consumption is equal to 1.59 mW. Further, the ideal and simulated gain- and phase-frequency characteristics for the filter are also demonstrated in Fig.14. It is obviously seen that the simulation results are in close agreement with the theoretically predicted values. In Fig.15, the simulated fast Fourier transform (FFT) frequency spectrum of the v_o signal is illustrated, where the total harmonic distortion (THD) for an input sinusoid of frequency 1.06 MHz is 0.275 %.

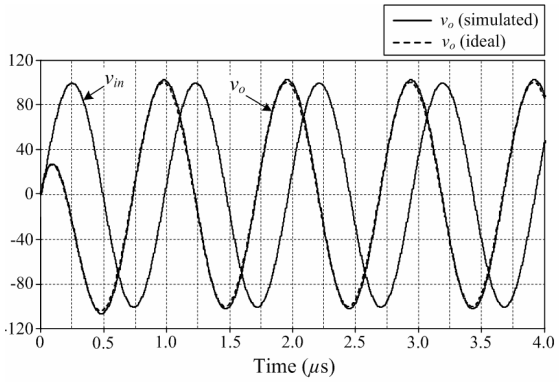

Fig. 13 – Time-domain responses for v_{in} and v_o waveforms of the all-pass filter in Fig.12.

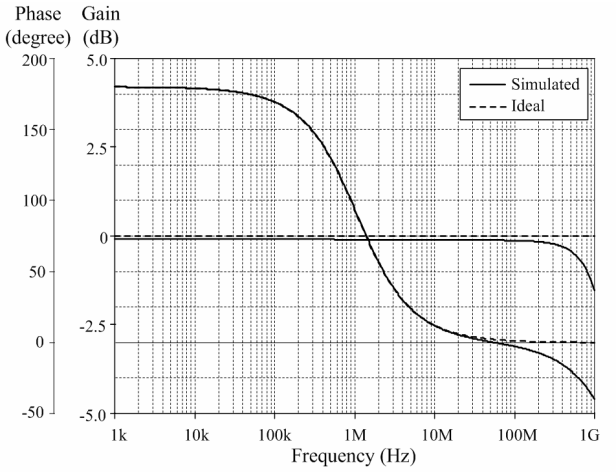

Fig. 14 – Gain- and phase-frequency responses of the all-pass filter in Fig.12.

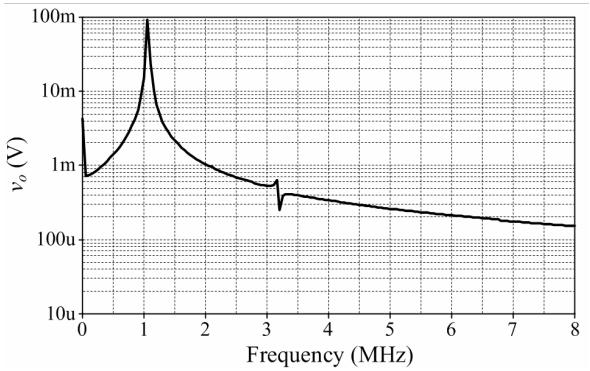

Fig. 15 – Simulated frequency spectrum for v_o at f_o = 1.06 MHz..

Next, the electronic tuning capability of the circuit is evaluated. For this purpose, the bias current I_B will set the values 20 μA, 26 μA, 38 μA, and 54 μA, resulting into values of g_m approximately equal to 250 μA/V, 330 μA/V, 500 μA/V, and 670 μA/V, respectively. For keeping the condition $g_m = 1/R$, the resistor R must respectively be of value 4 kΩ, 3 kΩ, 2 kΩ, and 1.5 kΩ. Fig.16 demonstrates the phase responses of the VDBA-based all-pass filter at four different values of I_B. It is noticed from Fig.16 that by tuning I_B the phase difference are approximately located 36 at°, 50°, 72°, and 89°, while the theoretically predicted values are 41°, 53°, 73°, and 90°, respectively.

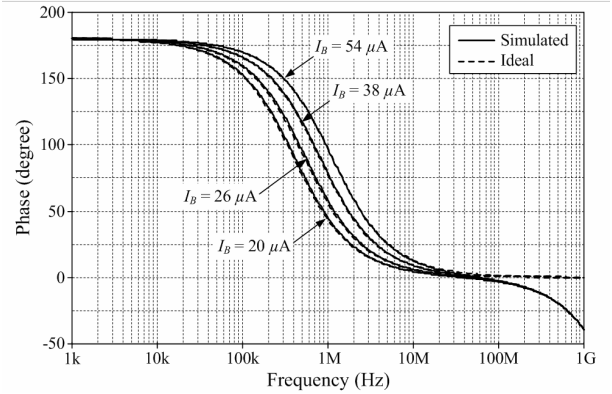

Fig. 16 – Simulated phase responses of Fig.12 with tuning I_B.

7. CONCLUSIONS

The circuit technique for designing linearly and electronically tunable CMOS VDBA with wide input voltage range is proposed. The design is based on a pair of differential-input amplifiers with active load and a current squarer. The basic function of the proposed VDBA has been tested in the realization of the electronically tunable first-order all-pass filter. Their performances have been verified by PSPICE simulation using 0.25 μm CMOS real process technology.

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