RESISTORLESS TUNABLE CAPACITANCE MULTIPLIER USING SINGLE VOLTAGE DIFFERENCING INVERTING BUFFERED AMPLIFIER

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Key words: Voltage differencing inverting buffered amplifier (VDIBA), Capacitance multiplier, Tunable circuits, Active filters.

The paper focuses on a novel configuration for the realization of the resistorless tunable grounded capacitance multiplier circuit using the newly introduced active building block called voltage differencing inverting buffered amplifier (VDIBA). The proposed capacitance multiplier circuit consists of only single VDIBA, one capacitor and one NMOS transistor acting as a voltage-controlled resistor (VCR). The equivalent capacitance value of the synthetic capacitor can be tuned electronically by adjusting the biasing current of the VDIBA and/or changing the control voltage of the VCR. To evaluate the behaviour of the circuit, an illustrative RC low-pass filter has been provided. Simulation results with TSMC 0.25 μm CMOS technology verify the theoretical analysis.

1. INTRODUCTION

For integrated circuit (IC) fabrication, it is a limiting problem to implement large-valued physical capacitors because of their disadvantageous in the usage of chip area, cost effectiveness, and tunability. For this reason, the design of a capacitance multiplication topology is advantageous from very large-scale integration (VLSI) implementation point of view. This is owing to the well-known fact that capacitance multiplication simulators help to realize higher equivalent integrated capacitors, avoiding the use of a large silicon chip space. In recent years, several methods for the implementation of the capacitance multiplication topologies using various active elements have been proposed in the technical literature [1–11]. In [1–4, 7–11], they contain two or more active components, which enlarge the chip size. Although the works presented in [5, 6–9] employ only a single active element, all the available realizations still use an excessive number of passive elements, at least three passive elements. Consequently, in the design of ICs, it is expected to realize capacitance multiplier circuits with a single active element and a minimum number of passive elements to simplify the circuit design. Recently, a new active building block called voltage differencing inverting buffered amplifier (VDIBA) has been introduced [12]. Even the internal structure of the just mentioned VDIBA is very simple when compared with other recently introduced active element counterparts. Its application universalities have been demonstrated on the design of several analog signal processing and signal generation circuits, such as a resistorless tunable voltage-mode first-order all-pass filter [12], triangle/square wave generators [13], voltage-mode universal biquad filters [14, 15], and synthetic lossy inductance simulators [16].

This work is focused on the realization of the grounded capacitance multiplier circuit using a VDIBA as an active element. The proposed synthetic capacitor is constructed with only a single VDIBA, one capacitor and one NMOS transistor working as an electronic resistor. The circuit has features of electronic tuning of its realized equivalent capacitance value and good sensitivity performance. The simulation results, obtained using PSPICE program, with

TSMC 0.25μm CMOS technology, verify the characteristics of the proposed circuit and its example application.

2. DESCRIPTION OF VDIBA

The electrical symbol of the VDIBA and its behavioural model can be represented in Fig.1a and 1b, respectively. Its port characteristics can be described by the following expressions:

$$i_p = i_n = 0 , \quad i_z = g_m(v_p - v_n) \quad \text{and} \quad v_{w-} = -v_z , \tag{1}$$

where g_m is the small-signal transconductance gain of the VDIBA. Since the transconductance gain g_m is usually controlled by electronic means trough the external dc bias current, this attractive feature makes the VDIBA device suitable for electronically tunable and resistorless circuit applications.
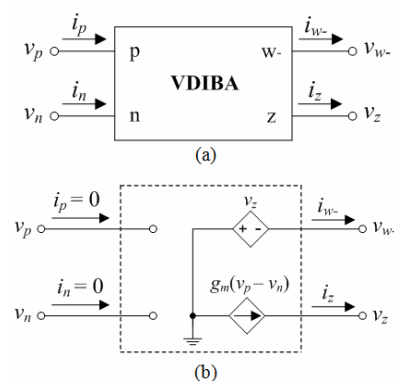

Fig. 1 – VDIBA; a) electrical symbol; b) its behavioural model.

According to Fig. 1, the VDIBA device has a pair of high-impedance voltage differencing inputs p and n, a high-impedance current output z, and a low-impedance inverting voltage output w−. The VDIBA is ideally composed of a differential-input operational transconductance amplifier followed by a unity-gain inverting voltage amplifier. The differential input voltage $(v_p - v_n)$ is converted to the output

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current flowing out at the terminal z (i_z) by a g_m parameter. The voltage drop at the terminal z (v_z) is then inverted and transferred to the output voltage at the terminal w– (v_{w-}).

The recent CMOS realization of the VDIBA is shown in Fig. 2 [12]. The input stage of the VDIBA comprises a differential pair with active load (M_1–M_4), which converts the differential input voltage (v_p– v_n) to the current i_z at the terminal z. For the output stage, transistors M_5–M_6 form the common-source amplifier with diode connected load, which provides $v_{w-} \cong -v_z$.
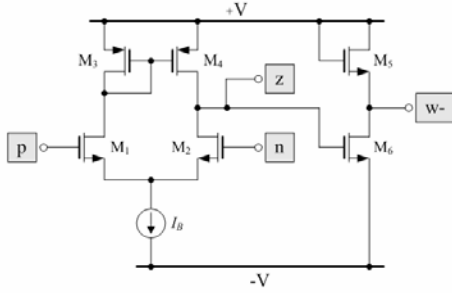

Fig. 2 – CMOS realization of the VDIBA.

3. PROPOSED CAPACITANCE MULTIPLIER CIRCUIT

The proposed electronically tunable and resistorless grounded capacitance multiplier circuit is shown in Fig. 3. It consists of only one VDIBA, one capacitor and one NMOS transistor (M_R). In this scheme, the transistor M_R is biased in triode region operation for acting like a voltage-controlled linear resistor (VCR). Its corresponding resistance value (R_{MOS}) can be given by:

$$R_{MOS} = \frac{1}{\mu_n C_{ox}\left(\dfrac{W}{L}\right)(V_C - V_{TH})}, \qquad (2)$$

where μ_n is the free electron mobility, C_{ox} is the gate-oxide capacitance per unit area, W and L are the effective channel width and length, V_{TH} is the threshold voltage of the transistor M_R, and V_C is an external dc control voltage used as a tool for tuning. Using (1) and deriving the proposed circuit of Fig. 3, its input impedance Z_{in} is realized of value:

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{sC_{eq}} = \frac{1}{s(1+g_m R_{MOS})C}. \qquad (3)$$
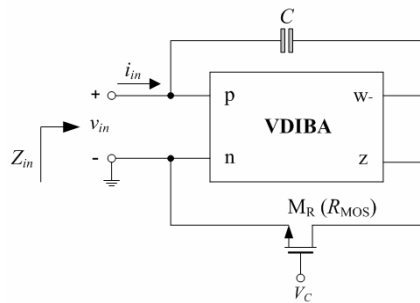

Fig. 3 – Proposed capacitance multiplier circuit.

It can easily be realized that the proposed circuit of Fig. 3 simulates a grounded capacitor with its equivalent capacitance value:

$$C_{eq} = (1 + g_m R_{MOS})C. \qquad (4)$$

The above expression demonstrates that the capacitance multiplication is feasible by electronically controlling the parameters g_m and/or R_{MOS}. In addition, no component matching constraint is required for its driving-point function realization.

4. NON-IDEAL GAIN EFFECT AND SENSITIVITY ANALYSIS

Under non-ideal condition, the voltage-current relationship of the VDIBA in (1) can be rewritten as :

$$i_p = i_n = 0 \ , \quad i_z = \alpha g_m (v_p - v_n)$$

and   (5)

$$v_{w-} = -\beta v_z \ ,$$

where $\alpha = (1 - \varepsilon_{gm})$ and $\beta = (1 - \varepsilon_v)$. Here, $|\varepsilon_{gm}| \ll 1$ represents the transconductance inaccuracy, and $|\varepsilon_v| \ll 1$ denotes the voltage tracking error from the terminal z to the terminal w–. Re-analysis of the proposed circuit of Fig. 3 by taking the VDIBA non-idealities into account, the value of C_{eq} for this case is found as:

$$C_{eq} = (1 + \alpha\beta g_m R_{MOS})C. \qquad (6)$$

From (6), it is clearly seen that the C_{eq} value of the simulator is affected by the non-ideal transfer gains of the VDIBA. However, this small discrepancy can be compensated by appropriately tuning the values of g_m and R_{MOS}.

The sensitivity analysis of (6) shows that the C_{eq} sensitivities with respect to active and passive components are obtained as:

$$S_{\alpha}^{C_{eq}} = S_{\beta}^{C_{eq}} = S_{g_m}^{C_{eq}} = S_{R_{MOS}}^{C_{eq}} = \frac{\alpha\beta g_m R_{MOS}}{1+\alpha\beta g_m R_{MOS}} < 1 \qquad (7)$$

and

$$S_C^{C_{eq}} = 1. \qquad (8)$$

All sensitivity figures are within unity in absolute value. This implies that the proposed capacitance multiplication simulator of Fig. 3 exhibits low active and passive sensitivities.

## 5. COMPUTER SIMULATION AND PERFORMANCE VERIFICATION

For the performance verification of the proposed capacitance multiplier realization in Fig. 3, the circuit has been simulated on PSPICE program with TSMC 0.25 μm CMOS process parameters. Some of the main technology parameters are as follows: threshold voltage $V_{TH} = 0.4238$ V, low field mobility $\mu_0 = 425.646$ cm^2/Vs, and gate oxide thickness $T_{ox} = 5.714$ nm for the NMOS transistor, and $V_{TH} = -0.5536$ V, $\mu_0 = 250$ cm^2/Vs, and $T_{ox} = 5.714$ nm for the PMOS transistor. In simulations, the VDIBA given in Fig. 2 was realized with dc supply voltages of $\pm V = \pm 0.75$ V. The dimensions of the MOS transistors are listed in Table 1.

Transistor	W (μm)	L (μm)
M_1 - M_2	2.5	0.25
M_3 - M_4	5.0	0.25
M_5 - M_6	75.0	0.25

The proposed capacitance multiplier of Fig. 3 was realized with the following component values: $I_B = 50$ μA ($g_m = 288$ μA/V), $C = 200$ pF and $R_{MOS} = 2.27$ kΩ realized with the M_R dimension equal to $W/L = 2.5/0.25$, and the external dc control voltage $V_C = 0.6$ V. This setting results in $C_{eq} = 0.303$ nF. Figure 4 shows the simulated time-domain responses for v_{in} and i_{in} of the grounded capacitance simulator in Fig. 3, where the applied frequency is $f = 100$ kHz. As measured in Fig. 4, there is a positive $86°$ phase shifting between v_{in} and i_{in}, which demonstrates that the proposed circuit works as a capacitance simulator. With the same component values, the simulated frequency responses for the input impedance Z_{in} of the capacitance multiplier of Fig. 3 together with the theoretical ones are also shown in Fig. 5. The total power consumption is recorded to be 5.27 mW.
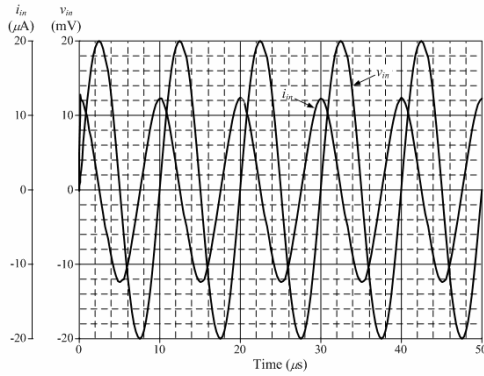

Fig. 4 – Simulated waveforms of v_{in} and i_{in} for the proposed capacitance multiplier of Fig. 3.
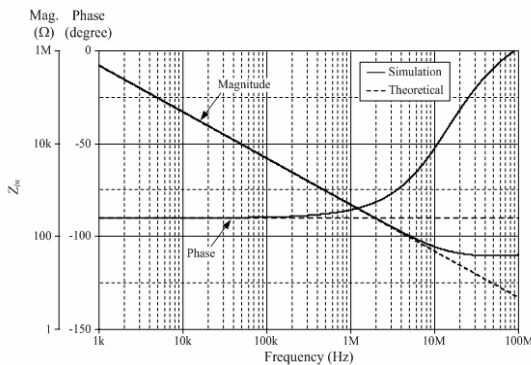
Fig. 5 – Simulated frequency responses for Z_{in} of the proposed capacitance multiplier of Fig. 3.

The capability of electronic adjustment of C_{eq} is demonstrated by performing simulations with a simultaneous change of I_B and V_C. Fig. 6 shows the magnitude-frequency characteristics of the input impedance for three different values of C_{eq}. The component values for tuning the C_{eq} value are given in Table 2. The obtained results are in close agreement with theoretical values approximately from 1 kHz to 5 MHz. Also from the results in Fig. 6, it is concluded that the circuit exhibits an electronically tunable capacitance over a wide range by tuning the values of g_m and V_C.

Table 2

Component values for C_{eq}-tuning in Fig. 6

	I_B (μA)	g_m (μA/V)	V_C (V)	R_{MOS} (kΩ)	C_{eq} (nF)
(i)	10	140	0.9	0.84	0.22
(ii)	100	383	0.6	2.27	0.37
(iii)	200	496	0.5	5.24	0.72
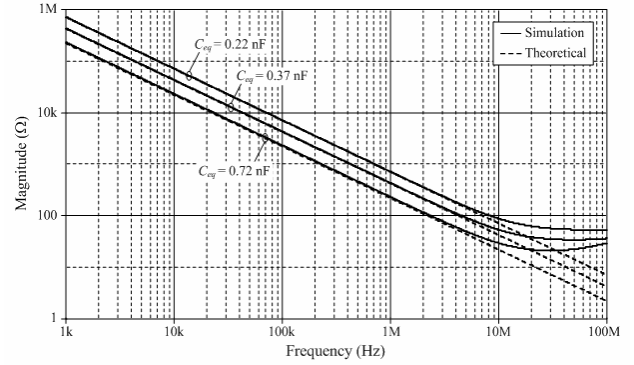
Fig. 6 – Magnitude-frequency characteristics for Z_{in} of the proposed capacitance multiplier, when tuning the value of C_{eq}.

To further demonstrate the workability of the proposed single VDIBA-based grounded capacitance multiplier realization of Fig. 3, it is constructed on a first-order RC low-pass filter shown in Fig. 7. The element values of an example filter are chosen as: $R_1 = 1$ kΩ and synthetic capacitors $C_{eq} = 0.22$ nF, 0.37 nF and 0.72 nF. The corresponding pole frequencies ($f_p = 1/2\pi R_1 C_{eq}$) are obtained at: $f_p \cong 752$ kHz, 430 kHz and 221 kHz, respectively. Both theoretical and simulated frequency responses of the low-pass filter in Fig. 7 are shown in Fig. 8.
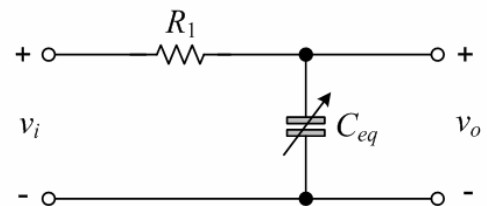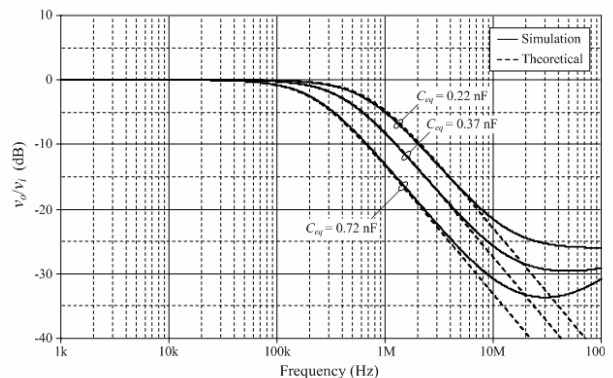

Fig. 7 – RC low-pass filter using the proposed capacitance multiplier of Fig. 3.
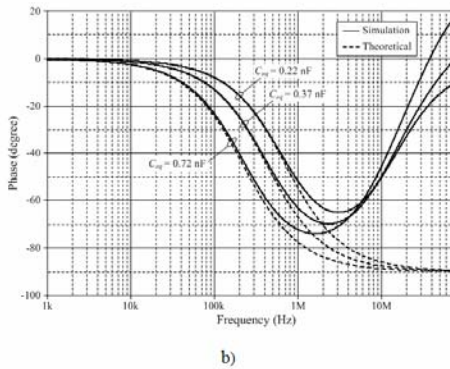

a)

Fig. 8 – Theoretical and simulated frequency responses
of the low-pass filter in Fig. 7: a) gain characrteristics;
b) phase characteristics.

6. CONCLUSIONS

An alternative solution for implementing an electronically tunable and resistorless grounded capacitance multiplier is introduced. The synthetic capacitor is made up of a single VDIBA together with one external capacitor and one electronic MOS resistor, and has been designed to operate with low-supply voltages of ±0.75 V. The value of the realized equivalent capacitance can be adjusted electronically. The circuit also provides the low-sensitivity performance with respect to the tracking errors of the VDIBA. The usability of the proposed circuit has been demonstrated on the first-order RC low-pass filter realization. Simulation results with TSMC 0.25 μm CMOS process parameters have been provided to validate the performance of the proposed capacitance multiplier circuit and its filter realization.

ACKNOWLEDGEMENTS

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