DESIGN OF LOSSLESS GROUNDED NEGATIVE INDUCTANCE SIMULATOR USING SINGLE OPERATIONAL TRANSRESISTANCE AMPLIFIER

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Key words: Grounded lossless inductance, Negative inductance simulation, Operational transresistance amplifier (OTRA).

In this paper a novel lossless grounded negative inductance simulator is proposed using only one operational transresistance amplifier (OTRA) as an active element and one capacitor and three or four resistors as passive elements. All the properties of the proposed negative inductance simulator are verified using both CMOS and current feedback operational amplifier (CFOA) based OTRA realization is PSPICE. The proposed circuit is also tested experimentally to verify the theoretical results. As an application, the cancellation of unwanted inductance is tested using the proposed inductance simulator.

1. **INTRODUCTION**

Although there are some feasible processes for fabrication of inductors as part of monolithic structure, still there arises some difficulty due to the particular spiral configuration of inductors, which occupy significant chip area and make them too costly and also suffer from substrate resistive losses and capacitive couplings. The process tolerances also lead to component variations, which cannot easily be tuned in passive case [1]. The disadvantages of passive inductor in Integrated Circuit have motivated the researchers to develop active inductor [2]. The positive inductance simulators find a wide range of applications, specially for the design of filter, oscillator, phase shifter and impedance matching circuits. Similarly the negative inductance simulator is equally useful for some applications such as cancellation of parasitic inductance, impedance matching [3] and generation of chaotic oscillation [4].

Recently Operational Transresistance Amplifier (OTRA) has emerged as an important current mode analog building block [5–6]. The input terminals of OTRA

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are internally grounded, thereby eliminating parasitic capacitances at the input. OTRA has the advantages of a high slew rate and wide bandwidth. It is a high gain current input voltage output device.

Some positive and negative grounded inductance simulator topologies using OTRA have been reported in [4, 7–12]. The topologies in [7–8, 11–12] and one circuit of [10] proposed lossless grounded inductance, but all of these circuits give positive inductance. The negative inductance simulator circuit proposed in [9] and [10] use one and two OTRA(s) as an active element respectively and three or four passive components; however none of these configurations can realize a lossless grounded inductance. Only the topology in [4] presents lossless grounded negative inductance simulator using single OTRA and some passive components.

In this work an attempt is made to propose a new lossless grounded negative inductance simulator employing single OTRA as an active element and some passive components. The proposed circuit is simulated in PSPICE using both CMOS based OTRA and current feedback operational amplifier (CFOA) based OTRA using macro model of AD844. The experiment is also performed for the proposed circuit using commercially available AD844AN. As an application, inductance balancing circuit is performed to display the workability of the proposed work.

2. **INDUCTANCE SIMULATOR**

The circuit symbol of an OTRA is shown in Fig. 1. The characteristic equations of this element can be described as

$$V_p = V_n = 0, \quad V_0 = R_m (I_p - I_n), \tag{1}$$

where, I_n, I_p, V_n, V_p are input currents and input voltages respectively at the n and p terminal of OTRA, R_m is transresistance gain of OTRA and V_0 is output voltage of OTRA. Fig.2 proposed the lossless grounded negative inductance simulator using OTRA.

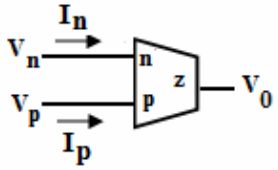


Fig.1 – Block diagram of OTRA.

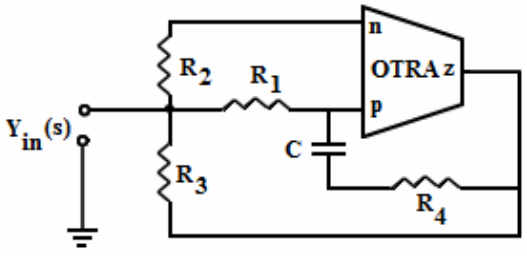


Fig. 2 – OTRA based proposed negative inductance simulator.

The routine analysis gives the equation for input admittance $\left[Y_{in}(s)\right]$ as

$$Y_{in}(s)=\frac{I_{in}(s)}{V_{in}(s)}=G_1+G_2+G_3+\frac{G_1G_3}{G_4}-\frac{G_2G_3}{G_4}+\frac{G_1G_3}{sC}-\frac{G_2G_3}{sC}, \tag{2}$$

where $I_{in}(s)$ is the input current, $V_{in}(s)$ is the input voltage, $G_1=\frac{1}{R_1}$, $G_2=\frac{1}{R_2}$, $G_3=\frac{1}{R_3}$, $G_4=\frac{1}{R_4}$, $s=\mathrm{j}\omega$.

If the condition $$G_1+G_2+G_3=\frac{G_3}{G_4}(G_2-G_1) \tag{3}$$

is satisfied, then $Y_{\mathrm{in}}(\mathrm{s})$ is purely inductive and the value of the negative inductance is $$L_{eq}=\frac{C}{G_3(G_2-G_1)}=\frac{CR_1R_2R_3}{R_2-R_1}. \tag{4}$$

On the other hand if $G_1 = 0$, the condition for lossless negative inductance is modified as $$G_2+G_3=\frac{G_2G_3}{G_4} \tag{5}$$

and the value of the inductance is $$L_{eq}=-\frac{C}{G_2G_3}=-CR_2R_3 . \tag{6}$$

Hence, it reveals that the circuit of Fig. 2 may be used to implement negative inductance with R_1 as well as without R_1.

The sensitivity of L_{eq} with respect to passive elements may be expressed as [13,14]

$$S_C^{L_{eq}}=S_{R_B}^{L_{eq}}=1,\ S_{R_1}^{L_{eq}}=\frac{R_1}{R_1-R_2},\quad S_{R_2}^{L_{eq}}=\frac{R_2}{R_2-R_1} \tag{7}$$

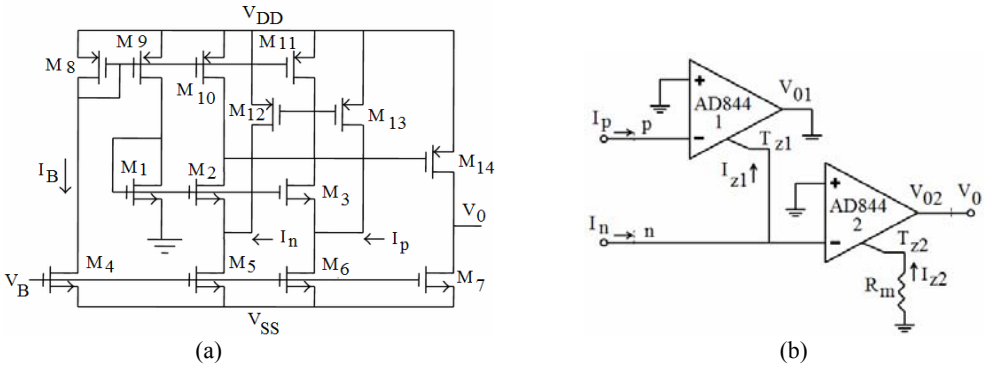
It shows that the sensitivity of the proposed circuit can be kept low.

3. **SIMULATION RESULTS**

To validate the theoretical prediction, the performance of the proposed inductance simulator is simulated using both CMOS and CFOA based OTRA in PSPICE. A CMOS based OTRA using 0.5 μm CMOS technology is given in Fig.3a [6] with DC power supply voltages $V_{\mathrm{DD}} = V_{\mathrm{SS}} = 1.5$ V and bias voltage $V_{\mathrm{B}} = –0.5$ V. Aspect ratios used for different transistors are same as [6]. For CFOA based implementation of the OTRA the macro model of the commercially available active device AD844 is used as shown in Fig.3b, with supply voltage of ± 5 V.

Inductance simulator of Fig. 2 is used to design L_{eq}= –10 mH using passive elements values as R_1 = 2 kΩ, R_2 = 1 kΩ, R_3 = 1 kΩ, R_4 = 5 kΩ and C = 5 nF. The ideal and simulated impedance magnitude for –10 mH inductance simulator is shown in Figs. 4.

It is well known that in a negative inductor current lead the voltage by 90°. To demonstrate this property of the negative inductance, a transient analysis is carried out for –10mH negative inductance using CFOA based OTRA. The passive components values are chosen as R_1 = 2 kΩ, R_2 = 1 kΩ, R_3 = 1 kΩ, R_4 = 5 kΩ and C= 5 nF with a sinusoidal input current signal of 10 μA peak value at 10 kHz. The simulation result is shown in Fig.5, where the current (I_L) lead the voltage (V_L) by 90° and the theoretical peak value for the voltage is calculated as 6.28 mV which is very close to the simulated value. Hence it reveals that the proposed circuit performs as a lossless grounded negative inductance simulator well.



(a) (b)

Fig. 3 – a) OTRA realization using CMOS [5]; b) OTRA realization using CFOA [3].

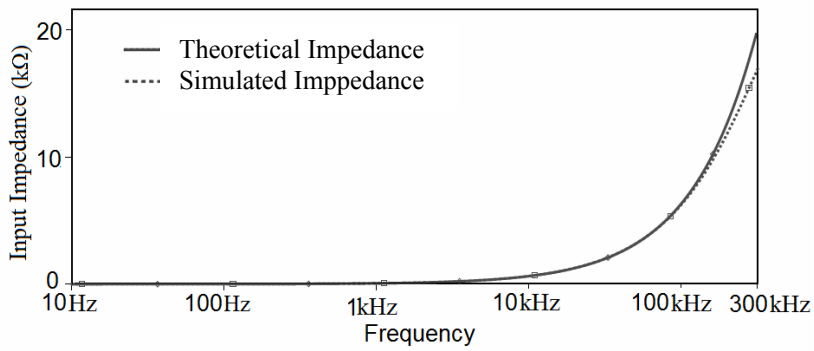


Fig. 4 – a) Impedance magnitude response of L_{eq} = –10 mH for CMOS based OTRA.

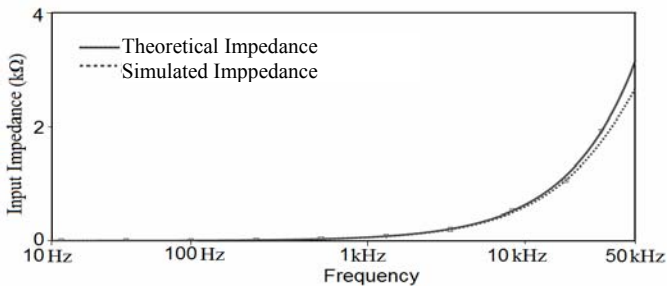


Fig. 4 – b) Impedance magnitude response of L_{eq} = –10 mH for CFOA based OTRA.

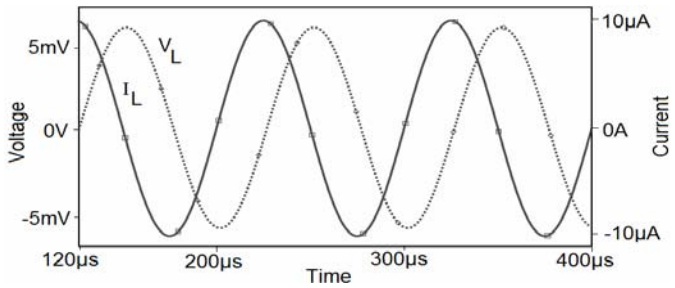


Fig. 5 – Voltage and current waveform for proposed negative inductance simulator of L_{eq} = –10 mH.

4. **EXPERIMENTAL VERIFICATION**

To verify the functionality of the proposed simulated inductance, the circuit is also experimentally tested. The experimental setup is shown in the Fig. 6 as that of reference [4]. The OTRA is constructed using commercially available AD844AN as shown in Fig. 3b [4] with a supply voltage of ± 5 V. A simulated negative inductance of value L = –4.16 mH is realized using R_1 = 1 kΩ, R_2 = 0.47 kΩ, R_3 = 0.47 kΩ, R_4 = 2.2 kΩ and C = 10 nF. To test the performance of the proposed circuit, 10 V_{PP} triangular voltage (V_{in}) is applied through R_{eq} = 1 kΩ resistor (to represent a triangular current source of 10 mA_{PP} with R_{in} = 10 kΩ inner resistance) as carried out in [15]. The input and output waveforms observed in the oscilloscope are shown in the Fig. 7. It is observed that the output (square wave) is of 1.2 V in comparison to the theoretical value of 1.3 V. The small deviation in experimental result is due to component tolerance of ± 10% as used in experiment (R_1 = 0.98 kΩ, R_2 = 0.464 kΩ, R_3 = 0.466 kΩ, R_4 = 2.22 kΩ, C = 10.1 nF). It is also observed that output voltage (square wave) lags the current (triangular wave) by 90°. Therefore, the experimental result also verifies that the proposed circuit performs well as negative inductance simulator.

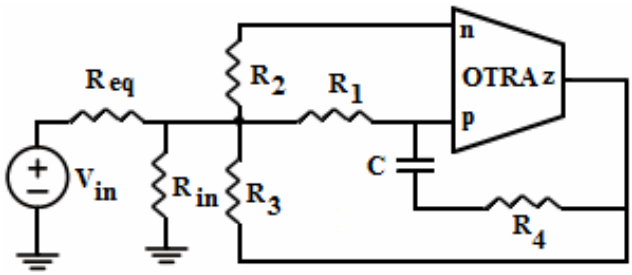


Fig. 6 – Experimental setup using AD844AN.

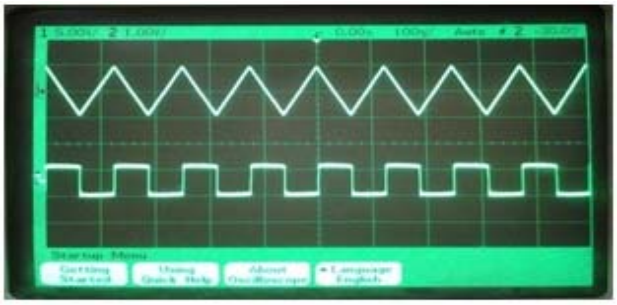


Fig. 7 – Experimental input (triangular waveform 5 V/div) and output (square waveform 1 V/div) waveforms in the proposed simulated inductance (time/div = 100 μs).

5. **APPLICATION**

To test the workability of the simulated negative inductance, an inductance compensation circuit is demonstrated which is shown in the Fig. 8, where a resistor (R) of 1 kΩ in series with positive inductor (L) of 10 mH and a sinusoidal input signal of amplitude (V_{in}) 10 mV at 10 kHz frequency is applied. To balance the effect of the positive inductance, the proposed negative inductance simulator (L_{eq}) of –10 mH is connected in series. When the circuit is simulated without the resistor (R) and positive inductor (L) then it simply acts as negative inductance circuit and the output of which is previously shown in Fig. 5 and discussed in simulation and results section. When the resistor (R) and positive inductor (L) are connected, the transient response gives the waveform as shown in Fig. 9. It is observed that the input voltage (V_{in}) and current (I_{in}) are in phase as the positive inductance in the circuit has been nullified by the simulated negative inductance, making the circuit purely resistive.

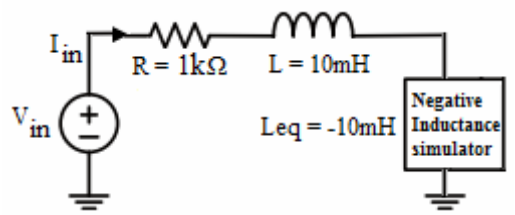


Fig. 8 – Inductance cancellation circuit using proposed negative inductance simulator.

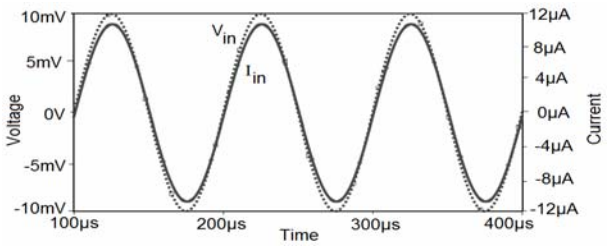


Fig. 9 – Transient response of the inductance cancellation circuit with L= +10 mH and L_{eq}= –10 mH.

6. **COMPARISON**

Table 1 shows the comparison of the proposed lossless grounded negative simulated inductance with the previously reported lossless/lossy grounded based on OTRA. The study of Table1 reveals that topologies presented in [7, 8, 11, 12] are lossless grounded simulated inductance, but all have positive value. Structure of [10] implements two circuits; one of them is lossless grounded positive inductance. The circuits [7, 8, 11, 12] use either excessive number or equal number of active and passive components as that of proposed one. The topologies of [4, 9] and one circuit of [10] implement negative grounded inductance. However inductance of [9, 10] are lossy. The circuit presented in [4] is only topology to implement lossless grounded negative inductance, which uses same number of active components and equal number or one excess passive component in comparison to the proposed work.

Table 2 shows the comparison in terms of frequency range of operation, power consumption and area consumed (in terms of no. of components) for the proposed inductance with all other circuits reported in [4, 7, 8, 10–12]. The comparison has been done for $\left|\pm L_{eq}\right|$ = 1 mH because of the availability of relevant data at that value of inductance using CFOA based OTRA realization. It is observed that proposed circuit outperforms both in terms of frequency range and

power consumption. The components required for implementing an inductance value of $|\pm L_{eq}|$=1mH are given in last column of Table 2. It shows that the proposed circuit and [4] perhaps consume the same chip area in terms of components used which is minimum in comparison to all other circuits except lossy grounded negative inductance topology of [9].

Table 1

Comparison of inductance simulator using OTRA

Ref.	Technology used for OTRA	Supply voltage for OTRA	No. of transistors for inductor implementation	No.of active component OTRA(s)	No. of passive components	Type of simulated inductor
[4]	Bipolar Junction Transistor (BJT) (AD844)	-	36	1	4 or 5 or 6	Lossless grounded negative L
[7]	BJT (AD844)	±5V	36	1	4	Lossless grounded positive L
[8]	0.5µm CMOS technology	±1.5V	28	2	6	Lossless grounded positive L
[9]	1.2µm CMOS technology	±5V	19	1	4	Lossy grounded negative L
					3	
[10]	BJT (AD844)	±10V	72	2	6	Lossless grounded positive L
					5	Lossy grounded negative L
[11]	CMOS technology	±2.5V	34	2	6	Lossless grounded positive L
[12]	0.5µm CMOS technology	±1.5V	14	1	5	Lossless grounded positive L
Proposed work	BJT (AD844)	±5V	36	1	4 or 5	Lossless grounded negative L
	0.5µm CMOS technology	±1.5V	14			

Table 2

Useful frequency range, power consumption and area (in terms of components) for ±1mH* inductance simulator

Ref	CFOA based OTRA realization		Components used $\left\|\pm L_{eq}\right\|$ = 1 mH for implementation
	Frequency range	Power consumption	
[4]	250 Hz – 350 kHz	0.262W	OTRA: One, Capacitor: One(3nF) Resistors: Five(1k,1k,1k,1.5k,3k) or Three or Four
[7]	200 Hz – 100 kHz	0.53W	OTRA: One, Buffer: One, Capacitor: Two(1nF,1nF),Resistors: Two(1k,1k)
[8]	200 Hz – 100 kHz	0.53W	OTRA: Two, Capacitor :One(3nF) Resistors: Five(1k,1k,1k,1k,3k)
[10]	150 Hz – 30 kHz	0.553W	OTRA: Two, Capacitor: One(1nF) Resistors: Five(1k,1k,1k,1k,4k)
[11]	150 Hz – 100 kHz	0.533W	OTRA: Two, Capacitor: One(1nF) Resistors: Five(1k,1k,1k,1k,3k)
[12]	200 Hz – 100 kHz	0.26W	OTRA: One, Capacitor Two(1nF,3nF) Resistors: Three(1k,1k,1k)
proposed	100 Hz – 400 kHz	0.12W	OTRA: One, Capacitor: One(0.5nF) Resistors: Four(2k,1k,1k,5k) or Three

**Note*. Comparison has been done for $\left\|\pm L_{eq}\right\|$ = 1 mH because of availability of relevant data in some literature for CFOA based OTRA only.

7. **CONCLUSION**

In this paper a new lossless grounded negative inductance simulator using single operational transresistance amplifier is proposed which uses three or four resistors and one capacitor. Although components matching are required, the proposed circuit offers the following advantageous features: (i) it uses single OTRA, (ii) it has low output impedance, hence suitable for cascading, (iii) moreover the capacitor is virtually grounded, which ease the wery large scale implementation and (iv) it has wide frequency range of operation and low power consumption. To demonstrate some of the properties of the negative inductance, PSPICE simulations are performed using both CMOS and macro model of AD844. The workability of the proposed circuit has also been verified experimentally using commercially available AD844IC.

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