Rev. Roum. Sci. Techn.– Électrotechn. et Énerg.
Vol. **64**, *4*, pp. 377–382, Bucarest, 2019

SYSTEMATIC SYNTHESIS FOR SECOND GENERATION CURRENT CONTROL CONVEYOR-BASED ADMITTANCE CONVERTERS

YONGAN LI, BO CHEN

Key words: Admittance converter, Second generation current control conveyor, Nodal admittance matrix expansion.

To synthesize admittance converter circuits employing the second generation current control conveyor (CCCII), based on the nodal admittance matrix (NAM) of the admittance converter, 16 pathological models of the positive and negative admittance converters are respectively synthesized by means of NAM expansion. The synthesized positive and negative admittance converters, using CCCIIs, have 16 different forms, respectively. These converters employ canonic number of components and are easy for the integrated circuit realization. Their parameters can be electronically tuned through tuning bias currents of CCCIIs. Finally, in order to verify the validity of the derived converters, the paper-and-pencil analyses are introduced. Moreover, a negative resistance oscillator is designed by employing a negative admittance converter and a positive admittance converter. The Multisim simulation results are in good agreement with the synthesis approach.

1. INTRODUCTION

An admittance converter is a basic circuit, which is widely used in communication, instrument, measurement and power electronic system. There are two types of the admittance converter circuits, one is the positive admittance converter, and the other is the negative admittance converter. The former can be used to simulate frequency-dependent elements such as inductances and frequency-dependent negative resistances for use in active filter synthesis. The latter can be used to neutralize unwanted ordinary resistances, as in the design of current sources, or control pole location, as in the design of active filters and oscillators. Based various active devices, such as the second generation current conveyor (CCII), operational transconductance amplifier, current follower transconductance amplifier, current controlled current conveyor transconductance amplifier, current controlled current differencing transconductance amplifier, current controlled current differencing buffered amplifier etc., a vast array of the admittance converter circuits have been developed [1–13]. Unfortunately, the most design methods for admittance converter circuits are not typical of systematic synthesis. Although the literature [1] provides a systematic synthesis approach for CCII based admittance converters, the synthesized circuits are unable to be controlled electronically. So far, the systematic synthesis approach about admittance converters employing the second generation current control conveyor (CCCII) has not been developed. Consequently, this problem is worth further research.

Our primary objective in this work is to use the nodal admittance matrix (NAM) expansion method to synthesize admittance converter circuits employing CCCIIs such that a circuit designer who understands the method well has more degree of freedom in the control and synthesis of new active circuits [14–20]. First, based on the NAM of the admittance converter, 16 pathological models of the positive and negative admittance converters are respectively obtained by means of NAM expansion, thereby producing 16 different forms of the positive and negative admittance converters using CCCIIs, respectively. Having used canonic number of components, the circuits are easy for the integrated circuit realization and the parameters of the converters can be electronically tuned through tuning bias currents of the CCCIIs. Next, the paper-and-pencil analyses are introduced to verify the validity for the synthesized admittance converters. Finally, in order to verify the realizability of the derived converters, a negative resistance oscillator is designed by employing a negative admittance converter and a positive admittance converter. The Multisim simulation results confirm the feasibility of the synthesize admittance converters and are in good agreement with synthesis method.

2. NAM EQUATION OF THE ADMITTANCE CONVERTERS

The literature [1] has given the NAM equation of the negative admittance converters as follows

$$G_n = -\frac{G_1 G_3}{G_2}. \tag{1}$$

After applying pivotal expansion, the equation (1) propagates the two NAM equations:

$$\boldsymbol{G}_n = \begin{bmatrix} 0 & G_3 \\ G_1 & G_2 \end{bmatrix}, \tag{2a}$$

$$\boldsymbol{G}_n = \begin{bmatrix} 0 & -G_3 \\ -G_1 & G_2 \end{bmatrix}. \tag{2b}$$

The NAM equation of the positive admittance converters has also been given by the literature [1]:

$$G_p = \frac{G_1 G_3}{G_2}. \tag{3}$$

Applying pivotal expansion to the equation (3) would propagate the following NAM equations:

$$\boldsymbol{G}_p = \begin{bmatrix} 0 & G_3 \\ -G_1 & G_2 \end{bmatrix}, \tag{4a}$$

$$\boldsymbol{G}_p = \begin{bmatrix} 0 & -G_3 \\ G_1 & G_2 \end{bmatrix}. \tag{4b}$$

School of Physics and Electronic Engineering, Xianyang Normal University, Xianyang 712000, China
E-mail: lya6189@tom.com.

Expanding NAM equation (3) will obtain the negative admittance converters, while expanding NAM equation (4) will obtain the positive admittance converters. As we proceed, we shall make frequent use of these equations.

3. CIRCUIT SYNTHESIS

3.1 SYNTHESIS FOR NEGATIVE ADMITTANCE CONVERTER

Starting from the matrix (2a) and inserting three blank rows and columns to adapt to requirement for the expanded matrix, first step to expand the matrix is employing a first nullator to connect columns 1 and 3, thereby shifting G_1 to the position 1, 3; then employing a first norator to connect rows 2 and 3, moving G_1 to the position 3, 3. Second step is adding a second nullator to link columns 2 and 4, thereby shifting G_2 to the position 2, 4; then adding a second norator to connect rows 2 and 4, moving G_2 to the position 4, 4. Third step is using a third nullator to connect columns 2 and 5, thereby shifting G_3 to the position 1, 5; then using a third norator to connect rows 1 and 5, moving G_3 to the position 5, 5. Shown in (5) is the expanded matrix, which includes nullor-mirror elements represented by bracket notation.

$$\boldsymbol{G}_n = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & 0 & G_3 \end{bmatrix}. \tag{5}$$

Here, a bracket in the horizontal direction denotes a nullator, a bracket in the vertical direction denotes a norator. Also, the sequence of expanding is from the inside to the outside. G_1, G_2, and G_3 are the admittances between nodes 3, 4, 5 and ground, respectively.

We see from (5) that this expanded matrix contains three pairs of pathological elements and three grounded admittances, namely G_1, G_2, and G_3.

Described in Fig. 1(a) is the physical model constructed by (5).

It should be emphasized here that applying all possible combinations of the added nullor-mirror elements will yield eight different forms of the expanded matrixes, thereby giving rise to eight different forms of the related physical models, as given in Fig. 1(a)–(h). From four the nullor-mirror models of the CCCII [16], we can also obtain eight CCCII implementation, as described in Fig. 2(a)–(h), which employ z_-–output CCCII (CCCII-) or inverting z_+–output CCCII (ICCCII+) or combination of both of them, where

$$\begin{aligned} G_1 &= 2I_{B1} / V_T, \\ G_2 &= 2I_{B2} / V_T, \\ G_3 &= 2I_{B3} / V_T. \end{aligned} \tag{6}$$

Here, I_{B1}, I_{B2}, and I_{B3} are the dc bias currents of CCCIIs, V_T is the thermal voltage.

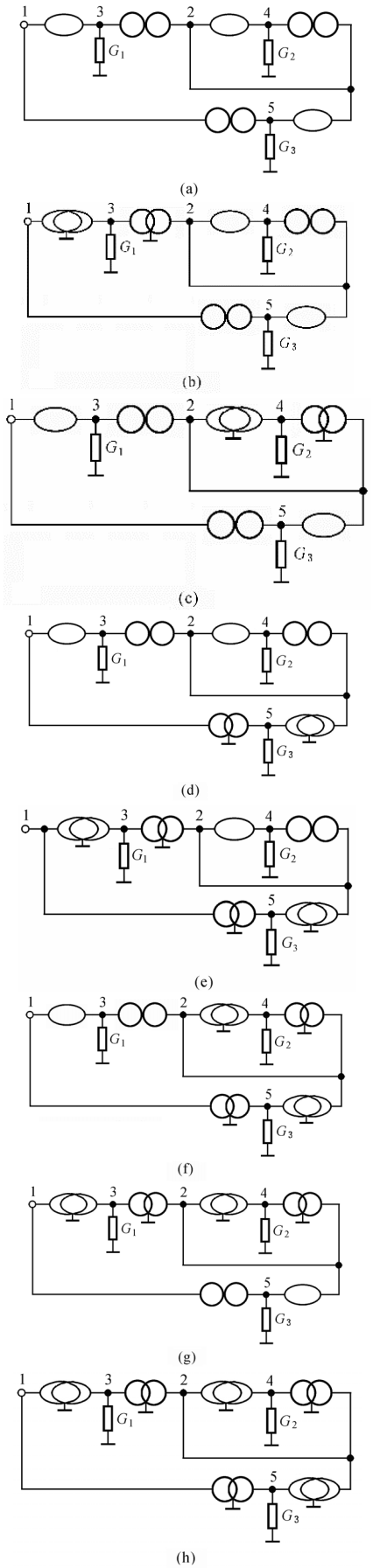
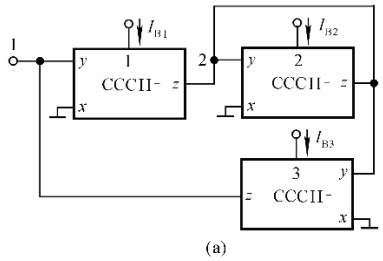


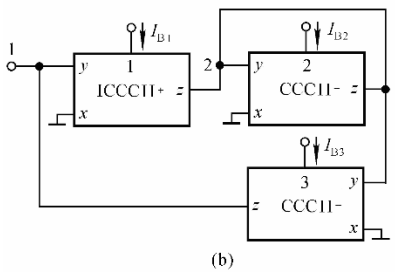
Fig. 1 – Physical models formed expanding (2a), (a) using three nullators and three norators, (b)-(d) using two nullators, two norators, one voltage mirror, and one current mirror, (e)-(g) using one nullator, one norator, two voltage mirrors, and two current mirrors, (h) using three voltage mirrors, and three current mirrors.

Similarly, begin from (2b), and applying all possible combinations of the added nullor-mirror elements will yield eight different forms of the expanded matrixes. Given in matrix (7) is one of them. The rest is omitted. In the (7), bracket in the horizontal direction denotes a nullator, a bracket in the vertical direction denotes a norator, and an angle bracket in the vertical direction denotes a current mirror.

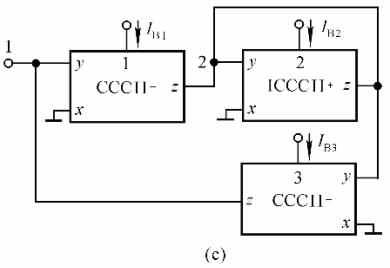
Described in Fig. 3 is one of eight related physical models. Indicated in Fig. 4 is one of eight related CCCII implementations, which may employ two types or three types of four forms of the CCCII. We then see that the negative admittance converter possesses 16 different forms.



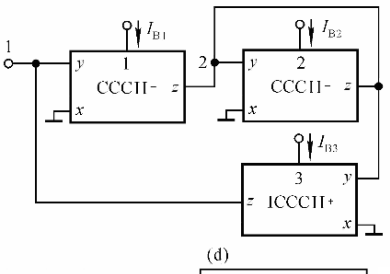
(a)



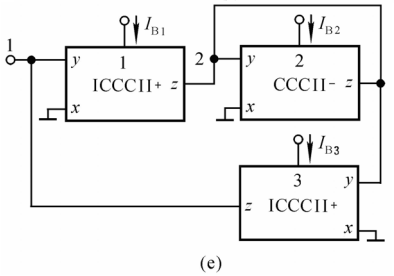
(b)



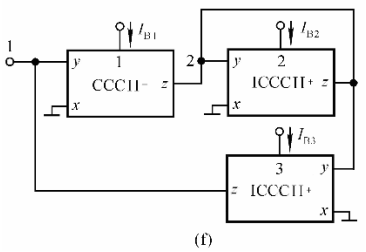
(c)



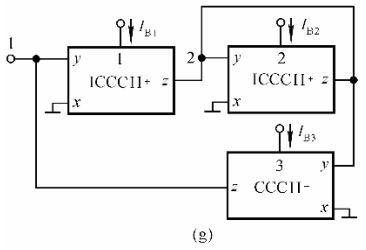
(d)



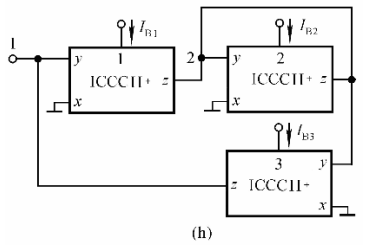
(e)



(f)



(g)



(h)

Fig. 2 – CCCII implementations of models in Fig.1.

$$\boldsymbol{G}_{\mathrm{n}} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & 0 & G_3 \end{bmatrix}. \tag{7}$$

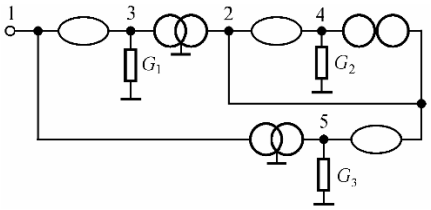


Fig. 3 – One of eight physical models formed expanding (2b).

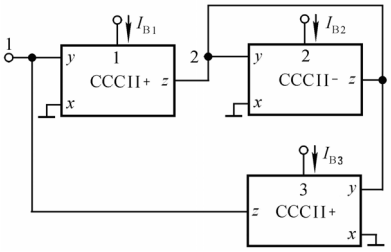


Fig. 4 – One of eight CCCII implementations of models in Fig. 3.

3.2 SYNTHESIS FOR POSITIVE ADMITTANCE CONVERTER

Begin from (4a), following successive steps as in the previous section, we can obtain eight expanded matrixes. Given in matrix (8) is one of them. The rest is omited.

Described in Fig. 5 is one of eight related physical models. Indicated in Fig. 6 is one of eight related CCCII implementations, which may employ two types or three types of four forms of the CCCII.

Similarly, beginning from (4b), we can obtain eight expanded matrixes. Given in matrix (9) is one of them. The rest is omited.

$$\boldsymbol{G}_p = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & 0 & G_3 \end{bmatrix}. \tag{8}$$

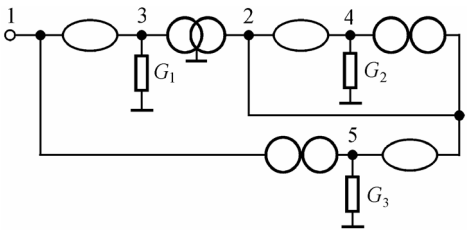


Fig. 5 – One of eight physical models formed expanding (4a).

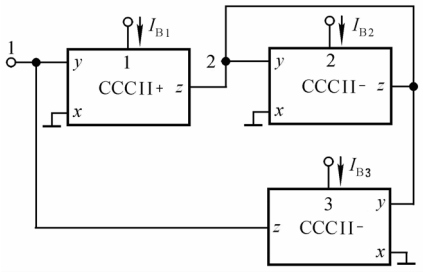


Fig. 6 – One of eight CCCII implementations of models in Fig. 5.

$$\boldsymbol{G}_p = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & 0 & G_3 \end{bmatrix}. \tag{9}$$

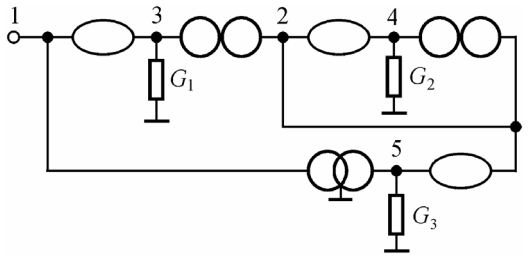


Fig. 7 – One of eight physical models formed expanding (4b).

Described in Fig. 7 is one of eight related physical models. Indicated in Fig. 8 is one of eight related CCCII implementations, which may employ two types or three types of four forms of the CCCII.

We then see that the positive admittance converter also possesses 16 different forms.

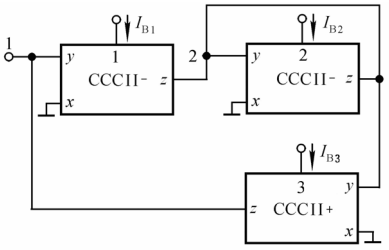


Fig. 8 – One of eight CCCII implementations of models in Fig. 7.

4. CIRCUIT ANALYSIS

It is well known that the circuit analysis is a reverse process of the circuit synthesis. So the validity for the synthesized admittance converter may be verified by the paper-and-pencil analysis. Let us first analyse the circuit of Fig. 2(a) in the negative admittance converter as an example. Inspecting the circuit of Fig. 2(a), we readily write equations as follows

$$I_{z1} = G_1 V_1, \quad V_{y3} = -I_{z1} / G_2, \quad I_1 = I_{z1} = G_3 V_{y3}. \tag{10}$$

Solving the above equations for I_1/V_1 and using (6), we have

$$G_n = \frac{I_1}{V_1} = -\frac{G_1 G_3}{G_2} = -\frac{2 I_{B1} I_{B3}}{V_T I_{B2}}. \tag{11}$$

It is obvious that this result is the same as (1).

Next, analysing the circuit of Fig. 6 in the positive admittance converter and inspecting the circuit of Fig. 2(a), we readily write the following equations:

$$I_{z1} = G_1 V_1, \quad V_{y3} = I_{z1} / G_2, \quad I_1 = I_{z1} = G_3 V_{y3}. \tag{12}$$

Solving the simultaneous equations, we obtain

$$G_p = \frac{I_1}{V_1} = \frac{G_1 G_3}{G_2} = \frac{2 I_{B1} I_{B3}}{V_T I_{B2}}. \tag{13}$$

It is obvious that this result is the same as (3). The analysis of the remaining circuits is omitted to limit the length of the paper.

It should be emphasized here that if I_{B2} is 10 μA, both I_{B1} and I_{B3} is 10 μA, 50 μA, 100 μA, the value of the synthesized admittance converter, from (11), is respectively –0.77 mS, -19.3 mS, -77 mS, which is much larger than the admittance converter formed by single CCCII.

5. DESIGN AND COMPUTER VERIFICATION

As an example of the admittance converter application, we design a negative resistance oscillator by using circuits of Fig. 2(a) and Fig. 6, as given in Fig. 9.

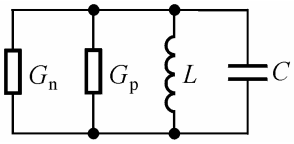


Fig. 9 – Negative resistance oscillator using CCCIIs.

The condition to occurs oscillation is that $|G_n|$ is greater than G_p. Using (10) and (12), we get

$$\frac{I_{nB1}I_{nB3}}{I_{nB2}} \geq \frac{I_{pB1}I_{pB3}}{I_{pB2}}. \quad (14)$$

The frequency to occurs oscillation is

$$f_o = \frac{1}{2\pi\sqrt{LC}}. \quad (15)$$

Set C as 100 pF, L as 1 mH, I_{nB2}, I_{nB3}, I_{pB2}, and I_{pB3} as 20 µA. When I_{nB1} is equal to 22 µA, which is greater than 20 µA of I_{pB1}, the condition for oscillation, from (14), is satisfied and the circuit will oscillate. The frequency of oscillation, from (14), is 500 kHz.

In order to confirm design results, we first establish the CCCII in NI MULTISIM by employing the transistor model of NR100N and PR100N. Then the circuit of Fig. 9, upon Fig. 2(a) and Fig. 6 was simulated with ± 2.5 V power supplies.

Shown in Fig. 10 is the *I-V* relationship of the negative admittance converter controlled by bias currents of the CCCIIs, where the slope of a straight line indicates negative conductance, which say that when I_{B2} is 10 µA, both I_{B1} and I_{B3} is set 10 µA, 50 µA, and 100 µA, the test values of the synthesized admittance converter are respectively –0.712 mS, –16.7 mS, and –60.2 mS.

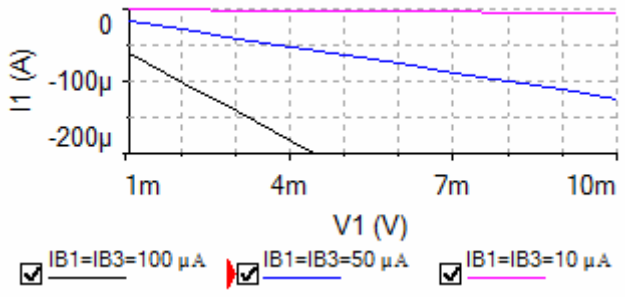


Fig. 10 – A graph of current versus voltage for three values of I_{B1} equal to I_{B3}, when I_{B2} is 10 µA.

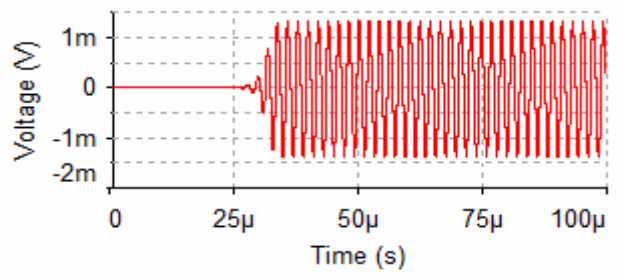


Fig. 11 – Initial transient response of the circuit in Fig. 9 for the design value of 500 kHz.

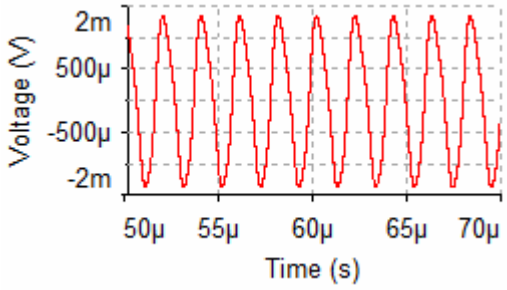


Fig. 12 – Expanded view of Fig. 11 after amplitude stabilization.

Shown in Fig. 11 is the initial transient response of the circuit in Fig. 9 for the design value of 500 kHz. Shown in Fig. 12 is the stationary oscillation response, which says that the circuit indeed oscillates. Using the cursors in MULTISIM yields the actual values for f_o is 483 kHz and the corresponding deviation for f_o is –4.2 %.

Shown in Fig. 13 is the Fourier analysis of the circuit in Fig. 9, which says that the total harmonic distortion is 4.6 % and the oscillator can produce sinusoidal signal with small distortion. Maximum power consumption is about 2.31 mW.

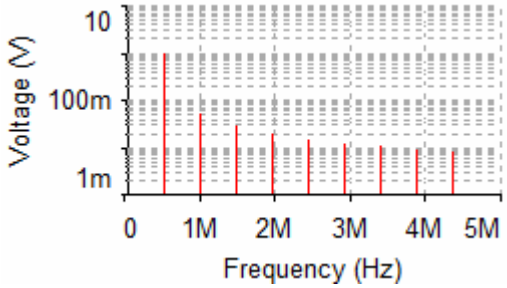


Fig. 13 – Simulation result of the output spectrum for the design value of 500 kHz.

It is noted that the circuit simulation's results are in agreement with theory.

6. CONCLUSIONS

In this paper, based on the NAM of the admittance converter, the admittance converter circuits employing CCCIIs are synthesized by means of NAM expansion, giving 16 pathological models of the positive and negative admittance converters, respectively. The synthesized positive and negative admittance converters, using CCCIIs, have 16 different forms, respectively. As an example to verify the oscillator is designed by employing a negative admittance converter and a positive admittance converter. Of course, if the oscillator's inductance is replaced by the simulation inductance using CCCIIs, one can also obtain electrical-variable-frequency oscillator by means of tuning bias currents of CCCIIs.

ACKNOWLEDGMENTS

This work is supported by Shaanxi Provincial Key Research and Development Program, China (Grant No. 2018NY-158). The author would also like to thank the anonymous reviewers for their suggestions.

Received on October 5, 2018

REFERENCES

1. A. M. Soliman, Generation and classification of CCII and ICCII based negative impedance converter circuits using NAM expansion, Int. J. Circuit Theory Appl., **39**, *8*, pp. 835–847 (2011).
2. A. M. Soliman, Generation *of generalized impedance converter circuits using NAM expansion*, Circuits Syst. Signal Process., **30**, *5*, pp. 1091–1114 (2011).
3. A. M. Soliman, *A note on the generation of generalized impedance converter circuits using NAM expansion*, Circuits Syst. Signal Process., **31**, *3*, pp. 1147–1157 (2012).
4. R. A. Saad, A. M. Soliman, *Generation, modeling, and analysis of CCII-based gyrators using the generalized symbolic framework for linear active circuits*, Int. J. Circuit Theory Appl., **36,** *3*, pp. 289–309 (2008).
5. R. A. Saad, A. M. Soliman, *On the systematic synthesis of CCII-based floating simulators*, Int. J. Circuit Theory Appl., **38**, *9*, pp. 935–967 (2010).
6. A. R. Hamad, M. A. Ibrahim, *Grounded Generalized Impedance Converter Based on Differential Voltage Current Conveyor (DVCC) and its Applications*, ZANCO Journal of Pure and Applied Sciences, **29**, *3*, pp. 118–127 (2017).
7. E. Yuce, S. Tokat, H. Alpaslan, *Grounded capacitor-based new floating inductor simulators and a stability test*, Turk. J. Electr. Eng. Co., **23**, *1*, pp. 2138–2149 (2015).
8. A. M. Soliman, *Three port gyrator circuits using transconductance amplifiers or generalized conveyors*, AEÜ-Int. J. Electron. Commun., **66**, *4*, pp. 286–293 (2012).
9. Y. A. Li, *NAM expansion method for systematic synthesis of OTA-based floating gyrators*, AEÜ-Int. J. Electron. Commun., **67**, *4*, pp. 289–294 (2013).
10. Y. A. Li, *A series of new circuits based on CFTAs*, AEÜ-Int. J. Electron. Commun., **66**, *7*, pp. 587–592 (2012).
11. Y. A. Li, *NAM expansion method for systematic synthesis of floating gyrators using CCCCTAs*, Analog Integr. Circuits Signal Process., **82**, *3*, pp. 733–743 (2015).
12. M. Siripruchyanun, W. Jaikla, CMOS current-controlled current differencing transconductance amplifier and applications to analog signal processing, AEÜ-Int. J. Electron. Commun., **62**, *4*, pp. 277–287 (2008).
13. S. Maheshwari, I. A. Khan, *Current controlled current differencing buffered amplifier: implementation and applications*, Active and Passive Electronic Components, **27**, *4*, pp. 219–227 (2004).
14. R. A. Saad, A. M. Soliman, *Use of mirror elements in the active device synthesis by admittance matrix expansion*, IEEE Trans. Circuits and Syst. I, **55**, *9*, pp. 2726–2735 (2008).
15. Y. A. Li, Y. H. Xi, Z. T. Fan, Y. Y. Zhang, J. X. Wu, *Systematic synthesis approach for floating gyrators employing single z-copy CCCCTA*, IET Circuits, Devices & Systems, **11**, *1*, pp. 41–45 (2017).
16. Y. A. Li, Modeling, *synthesis, analysis, and simulation of CCCII-based floating gyrators*, Analog Integr. Circuits Signal Process., **88**, *3*, pp. 443–453 (2016).
17. A. M. Soliman, C. M. Chang, *Generation of Four Phase Oscillators Using Op Amps or Current Conveyors*, Journal of Active & Passive Electronic Devices, **10**, *3–4*，pp. 207–221(2015).
18. Y. A. Li, *Synthesis of compact VDTA-based Wien oscillators with grounded capacitors*, AEÜ-Int. J. Electron. Commun., **84**, *2*, pp. 281–289 (2018).
19. L. Tan, Y. Wang, G. Yu, *Active filter synthesis based on nodal admittance matrix expansion*, EURASIP Journal on Wireless Communications and Networking, **2017**, *1*, pp. 96–106 (2017).
20. Y. A. Li, Y. H. Xi, Z. T. Fan, Y. Y. Zhang, J. X. Wu, *Systematic synthesis of second generation current-controlled conveyor-based Tow-Thomas filters with orthogonal tune of pole frequency and quality factor*, Rev. Roum. Sci. Techn.–Électrotechn. et Énerg., **62**, *1*, pp. 76–81 (2017).