

LOW VOLTAGE CHARGE PUMP CIRCUIT USING 0.18 μm CMOS TECHNOLOGY

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Key words: Charge pump, CMOS, EEPROM, NVM.

An enhanced charge pump circuit utilizing charge-transfer-switch (CTS) to direct charge flow with improved voltage pumping gain is proposed in this paper. The diode-configured output stage limitation is managed through the pumping of output stage by the clock of improved charge pump circuit. Using Mentor Graphics, the proposed charge pump circuit is designed in 0.18 μm CMOS process. It is able to pump an input voltage of 1.8 V to a measured output of 5.95 V through 20MHz clock signal with each pumping capacitor of 0.1 pF and smoothing capacitor of 0.1 pF at the output. From the simulation result, it is evident that the proposed charged pump circuit offers higher pumping gain compared with the existing charge pump circuit. Besides, using in Non-Volatile Memory (NVM), proposed design can be used in low voltage memory circuits.

1. INTRODUCTION

Charge pump circuits are extensively utilized in many applications due to its small power consumption, high performance, low current drivability and small area. Charge pump circuits pump charges upward to produce voltages higher than the regular supply voltage [1–5]. They are usually applied to the NVMs, such as Electrically Erasable Programmable Read-Only Memory (EEPROM) or flash memories, to erase or to write the floating-gate devices [6]. Embedded systems that have a stringent silicon estate need fully on-chip charge pumps [7]. Recently, embedded NVM has received much attention due to its utilization in Radio Frequency Identification (RFID) tag, System on Chip (SoC), microcontroller unit, FPGA systems etc.

For on-chip charge pumps, efficiency in power and area are two major concerns. Besides, fabrication of NVM requires special multipolysilicon processes and multioxidation for thin SiO₂ layers. Many masks are needed which result in lower yield, higher cost, lower reliability and longer process turnaround time compared to standard CMOS technology [8]. By taking the challenge, NVM is

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developed by many researchers in a standard CMOS logic process since it has the benefits of lower power dissipation [8–11]. On the contrary, the endurance and maintenance characteristics are unsatisfactory due to the single-ended memory cell architecture with a too thin oxide [10] or the nMOS tunneling junction [8]. With a higher bit per area, it consumes more power because every bit cell takes its own high voltage switch [9, 11]. Hence, an internal high voltage generator circuits such as charge pumps or voltage doublers are required to supply these high voltages [12–13].

Generally, charge pump circuit is capacitor based, where voltage is pumped-up at each stage depending on each stage voltage gain. Charge pump circuits are mostly based on Dickson charge pump circuit [14, 15]. Pumping capacitors and diode connected nMOS are major elements of this type of charge pump circuits. Since there are body effect of the nMOS and threshold voltage, the circuit needs to sustain large voltage loss, which leads to low voltage gain per stage. To develop higher pumping efficiency, charge pump circuit is modified by Jongshin *et al.* [16]. However, threshold voltage and parasitic capacitance are still limiting the pumping efficiency [17].

This paper proposes a higher pumping gain charge pump circuit for NVMs in four pumping stage and without any parasitic capacitor to reduce power dissipation.

2. ARCHITECTURE

In this section, the existing charge pump circuits, such as Mensi *et al.* [18] with new integrated charge pump architecture using dynamic biasing of pass transistors and Che *et al.* [19] with ultra-low-voltage low-power charge pump are discussed.

2.1. DYNAMIC BIASING OF PASS TRANSISTORS (DBPT)

The architecture is based on pMOS pass transistor by the dynamic biasing of bodies and gates. Voltage loss due to the device threshold is removed by controlling gate and body voltages of every pass transistor, leading to negligible voltage drop through each pumping stage.

In Fig. 1, the charge transfer block is behaving as a diode of the traditional Dickson charge pump. Similarly, the whole charge pump architecture is regulated by two complementary clock signals. The Charge Transfer MOSFET (CTM) active control is based on two auxiliary pMOS M_{b1} and M_{b2} . This active control can reduce the body effect onto the threshold voltage of each charge transfer block [18].

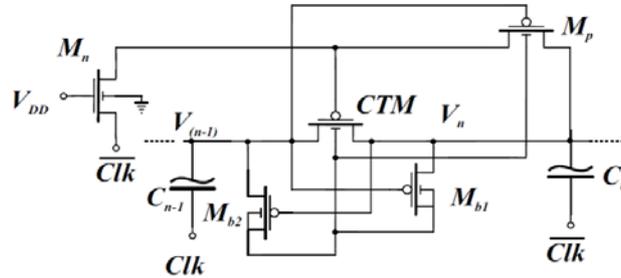


Fig. 1 – DBPT charge transfer block architecture per stage.

2.2. ULTRA-LOW-VOLTAGE LOW-POWER (ULVLP)

Che *et al.* proposed a new charge pump by utilizing two symmetrical branches and pMOS-only transfer transistors at each stage. Fig. 2 shows schematic of the proposed four-stage charge pump, which contains charge transfer branch A and branch B. The disparity between these two branches is the clock signals, where their phases are in opposite to each other. As such, symmetric nodes in branch A and B are charged alternately. Both of them have the similar amplitude but with opposite phase. In this design, there are two steps. The first part is by using the voltage difference of symmetrical nodes to control the transistors. To overcome the body effect, the second part is using only pMOS [19].

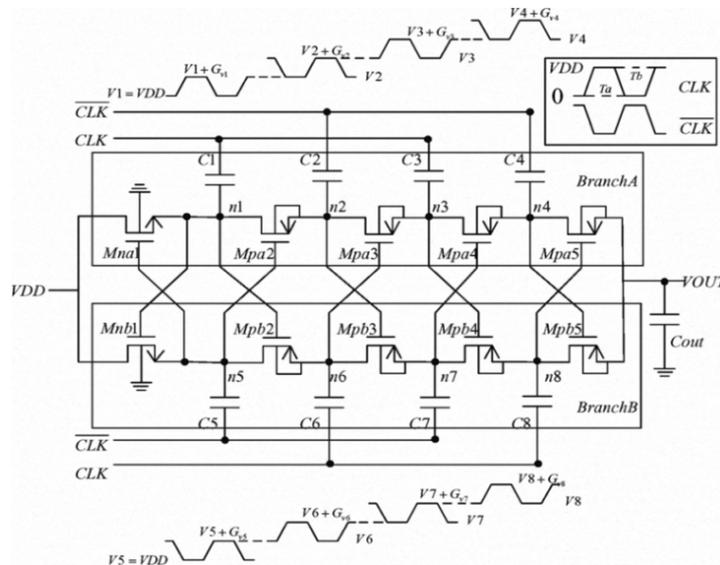


Fig. 2 – ULVLP four-stage charge pump architecture.

3. PROPOSED CHARGE PUMP CIRCUIT

In the proposed work, dynamic CTS method is used to reduce the body effect and the voltage loss problem of the previous research works. All diode-connected MOSFETs from MD1 to MD4 are used to set up the initial voltage as shown in Fig. 3. However, the MOSFETs (MD1-MD4) are not involved in the CTS control scheme. NMOS CTSs from MS1 to MS4 is used to control the switches. However, the switches (MS1-MS4) are not turned off completely during the charge transferring process. As a result, some voltage loss occurs. Therefore, pass transistors MNs and MPs are utilized to turn on/off dynamically the switches completely in order to prevent the voltage loss. Moreover, the backward control scheme is employed to derive high voltage from the previous stage. To boost up the gain, CLKA and CLKB clock signals are out-of-phase but with the amplitudes of VDD. The output voltage of the proposed circuit can be expressed as

$$\Delta V = V_{clk} \frac{C_{pump}}{C_{pump} + C_{par}} - \frac{I_o}{f \cdot (C_{pump} + C_{par})}, \quad (1)$$

where, V_{clk} is the voltage amplitude of the clock signals, C_{pump} is the pumping capacitance, C_{par} is the parasitic capacitance at each pumping node, I_o is output current, and f is the clock frequency.

For condition where CLKB is low and CLKA is high, voltages at both node 1 and 2 are the same as V_2 while voltage at node 3 is more than $2\Delta V$ of voltage at node 1, if

$$2\Delta V > V_{tp} \text{ and } 2\Delta V > V_m(V_2), \quad (2)$$

where V_{tp} is the threshold voltage of pMOS (MPs).

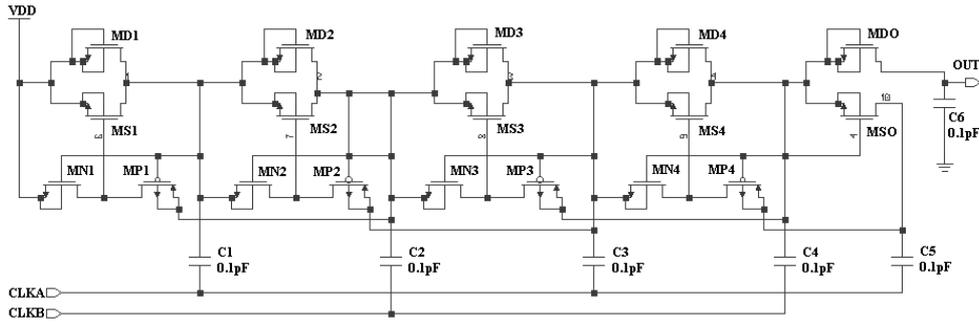


Fig. 3 – Proposed charge pump circuit schematic utilizing dynamic CTS.

By the voltage at node 3, both the MP2 and MS2 are turned on. MN2 is always off during this phase as the gate-to-source voltage is zero.

For condition where CLKA goes low and CLKB goes high, voltage at node 1 is V_1 . Both the voltages at node 2 and 3 are more than $2\Delta V$,

$$2\Delta V > V_{tn}(V_1), \quad (3)$$

where V_{tn} is the threshold voltage of nMOS (MNs).

Since MS2 is free from control of node 3, during this time, MN2 is switched on and MP2 is switched off. For the successful accomplishment of the operation, both the equation 1 and equation 2 are required. For each pMOS, drain node of every individual well is connected. During the short period of transition, the charges at the CTSs gate node can be injected into the well, when CLKA or CLKB goes from high to low.

4. SIMULATION RESULT

CEDEC 0.18 μ m CMOS process is used to verify the output results of the enhanced CP circuit with the ELDONET simulator. The transistors involved in the pumping circuitry are of equal size which is $W/L= 1.4 \mu/0.18 \mu$. Generally, the voltage amplitudes of CLKA and CLKB are same as power supply voltage (VDD). The simulation parameters used are at pumping clock frequency 20 MHz; pumping capacitor with 0.1 pF; smoothing capacitor with 0.1 pF; input voltage (VDD) ranged from 1.8 V to 3.3 V; number of pumping stages ranged from 2 stages to 8 stages.

Fig. 4 shows the output voltage for proposed charge pump schematics. It is observed that the proposed charge pump circuit can pump a low power supply voltage 1.8 V up to 5.95 V output voltages.

Comparison between proposed charge pump with existing charge pump is shown in Fig. 5. It is clear from Fig. 5 that the proposed charge pump circuit is giving the highest output voltage, which leads to higher pumping gain for each stage compared to the DBPT and ULVLP.

Besides, this research also shows simulated output voltages for comparing the performance of DBPT, ULVLP and proposed charge pump circuit corresponding to the number of stages. The comparison study between the output voltages and the number of stages among DBPT, ULVLP and this research work under 1.8 V as the VDD is listed in Table 1.

Table 1

Comparison study among DBPT, ULVLP and this research work

Number of Stages	DBPT [18] (voltage)	ULVLP [19] (voltage)	This Work (voltage)
2	3.9	3.8	3.9
4	4.8	3.9	5.9

Table 1
(continued)

Number of Stages	DBPT [18] (voltage)	ULVLP [19] (voltage)	This Work (voltage)
6	5	4.5	6.2
8	5.2	5.2	7.2

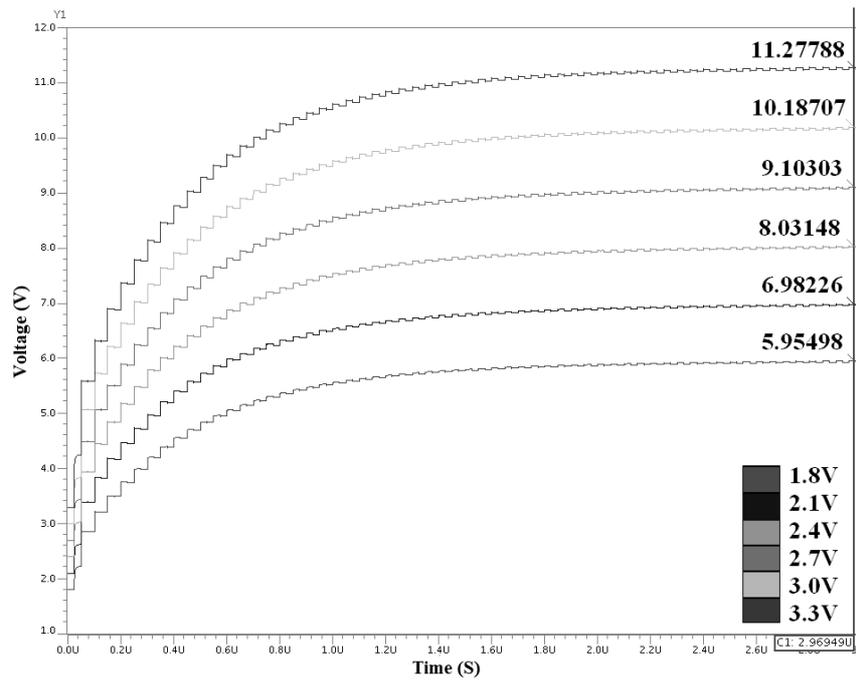


Fig. 4 – Output voltages for proposed charge pump schematics with $1.8\text{V} \leq \text{VDD} \leq 3.3\text{V}$.

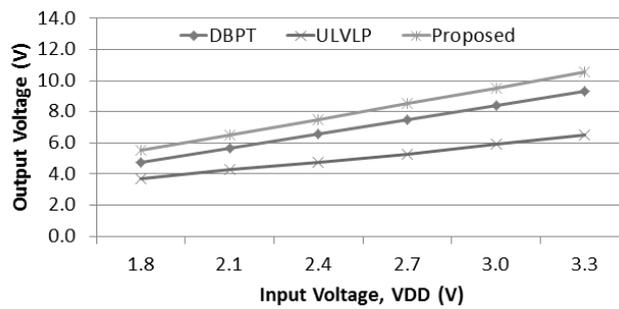


Fig. 5 – Simulated output voltages for four-stage charge pumps with $1.8\text{V} \leq \text{VDD} \leq 3.3\text{V}$.

Fig. 6 shows the layout design for proposed four-stage charge pump using CEDEC 0.18 μm CMOS technology. The size of the layout design is $40 \times 60 \mu\text{m}$. The layout is designed for the ease to cascade more pumping stage to the desired output voltage for further development. It is obvious from the Fig. 6 that, the designed charge pump circuit occupies only a small area, which eventually reduces the cost.

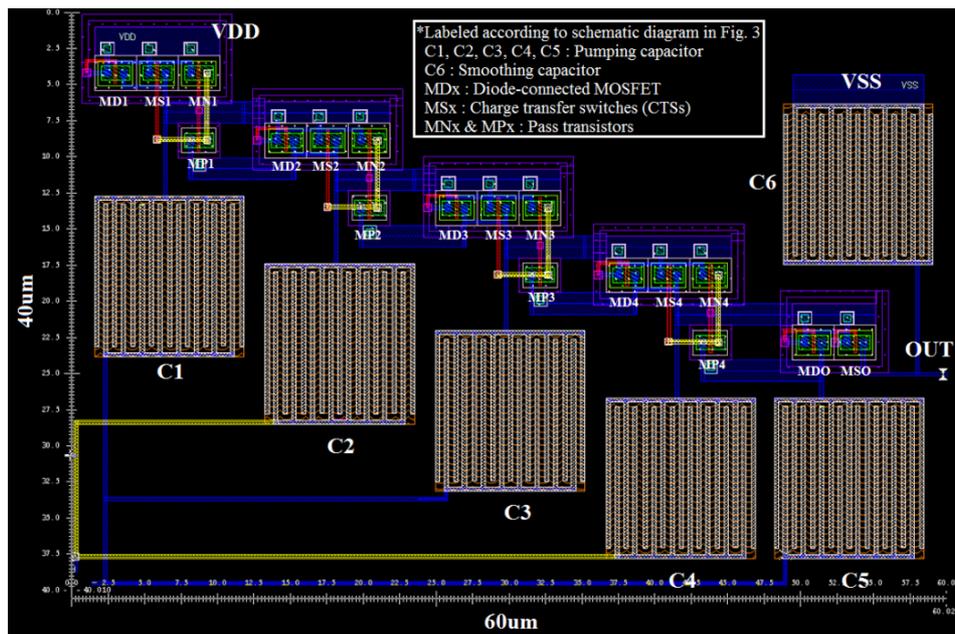


Fig. 6 – Layout design for proposed four-stage charge pump using CEDEC 0.18 μm CMOS technology.

Fig. 7 shows the post-layout simulation result of the proposed charge pump circuit. It is found from the post layout simulation that, under a low $V_{DD} = 1.8 \text{ V}$, the proposed circuit is pumping up to 5.07 V as the output voltage.

Typically, schematic simulation is considered ideal case while post layout simulation is considering the real case, which includes parasitic capacitance, reverse charge sharing or body effect. However, the post-layout simulation output voltage has been decreased 14% compared to the schematic simulation, which is shown in Fig. 8.

Therefore, all these components, lead to decrease the output voltages. Nevertheless, the proposed charge pump layout is able to boost up the voltage from 1.8 V to 5.07 V .

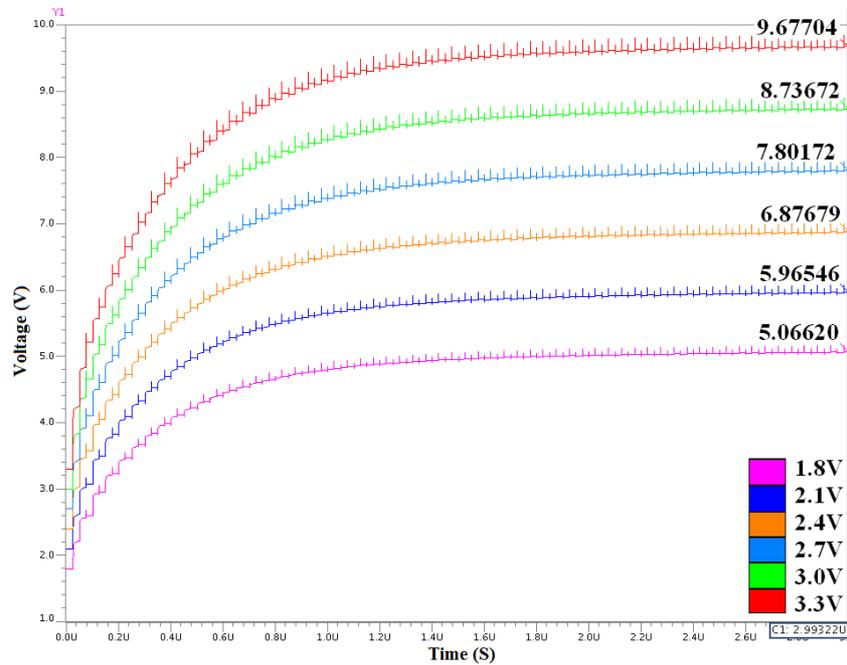


Fig. 7 – Output voltages for proposed four-stage charge pump layout design with $1.8V \leq VDD \leq 3.3V$.

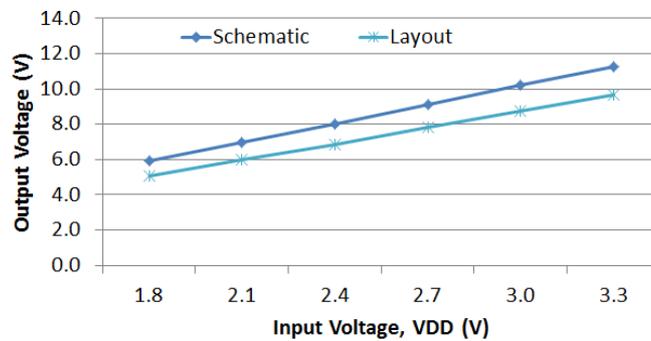


Fig. 8 – Comparison between schematic simulation and layout simulation for proposed four-stage charge pump with $1.8V \leq VDD \leq 3.3V$.

5. CONCLUSION

An enhanced charge pump circuit utilizing the CTS to direct charge flow with improved voltage pumping gain is proposed. The diode-configured output stage limitation is managed through the pumping of the output stage by the clock of

improved charge pump circuit. It is able to function in low-voltage memory devices with the least parasitic capacitance. The simulation result shows that the proposed charge pump circuit is capable of producing 5.95 V output for 1.8 V power supply voltage with each pumping capacitor of 0.1 pF. The charge pump circuit is suitable for memory circuits of low voltage applications.

Received on 12 June 2012

REFERENCES

1. Y. Wang and L. Ruzhang, *A feedback based charge pump*, IEEE International Conference on Anti-Counterfeiting, Security and Identification (ASID), Xiamen, China, 24–26 June 2011.
2. R. Aloulou, H. Mnif, F. Aicalapa and M. Loulou, *An improved MOS charge pump circuit for low voltage operations and wireless sensor applications*, International Conference on Microelectronics (ICM), 201, Hammamet, Tunisia, 19–22 December 2011.
3. O. Wong, W. Tam, C.Kok and H. Wong, Chi-Wah Kok; Hei Wong, *A low-voltage charge pump with wide current driving capability*, IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Hongkong, 15–17 December 2010,
4. M. Huang, P. Fan and K. Chen, *Low-Ripple and Dual-Phase Charge Pump Circuit Regulated by Switched-Capacitor-Based Bandgap Reference*, IEEE Transactions on Power Electronics, **24**, 5, pp. 1161–1172, (2009).
5. P. Feng; Y. Li and N. Wu, *An improved charge pump circuit for non-volatile memories in RFID tags*, 10th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2010, Shanghai, China, 1–4 November 2010.
6. K. Ming-Dou, C. Shih-Lun and T. Chia-Shen, *Design of Charge Pump Circuit With Consideration of Gate-Oxide Reliability in Low-Voltage CMOS Processes*, IEEE Journal of Solid-State Circuits, **41**, 5, pp. 1100–1107 (2006).
7. K. Wing-Hung, L. Yan, S. Feng and T. Chi-Ying, *Design and analysis of on-chip charge pumps for micro-power energy harvesting applications*, 19th IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC), 2011, Hong Kong, China, 3–5 October 2011.
8. K. Ohsaki, N. Asamoto and S. Takagaki, *A single poly EEPROM cell structure for use in standard CMOS processes*, IEEE Journal of Solid-State Circuits, **29**, 3, pp. 311–316, Mar. 1994.
9. D.X. Zhao, N.Y.W. Xu, L.W. Yang and J.Y. Wang, *Low-power, Single-poly, Non-volatile Memory for Passive RFID Tags*, Chinese Journal of Semiconductors, **29**, pp. 99–104 (2008).
10. B. Wang, H. Nguyen, Y. Ma and R. Paulsen, *Highly Reliable 90-nm Logic Multitime Programmable NVM Cells Using Novel Work-Function-Engineered Tunneling Devices*, IEEE Transactions on Electron Devices, **54**, 9, pp. 2526–2530 (2007).
11. J. Raszka, M. Advani, V. Tiwari, L. Varisco, N.D. Hacobian, A. Mittal, M. Han, A. Shirdel and A. Shubat, *Embedded flash memory for security applications in a 0.13 μm CMOS logic process*, Proceedings of the International Solid-State Circuits Conference (ISSCC), IEEE, Philadelphia, USA, 15–19 February 2004.
12. M.G. Mohammad, M.J. Ahmad and M.B. Al-Bakheet, *Switched positive/negative charge pump design using standard CMOS transistors*, IET Circuits Devices Syst., **4**, 1, pp. 57–66 (2010).
13. D. Somasekhar, B. Srinivasan, G. Pandya, F. Hamzaoglu, M. Khellah, T. Karnik and K. Zhang, *Multi-Phase 1 Ghz Voltage Doubler Charge Pump in 32nm Logic Process*, IEEE Journal of Solid-State Circuits, **45**, 4, pp. 751 (2010).
14. J.F. Dickson, *On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique*, IEEE Journal of Solid-State Circuits, **11**, 3, pp. 374–378, (1976).

15. W. Henru and C. Yuhua, *A charge pump circuit design based on a 0.35um BCD technology for high voltage driver applications*, Proceedings of the 9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT), California, USA, 30–23 October 2008.
16. J. Shin; I.Y. Chung; Y. J. Park; Hong and S. Min, *A new charge pump without degradation in threshold voltage due to body effect [memory applications]*, IEEE Journal of Solid-State Circuits, **35**, 8, pp. 1227–1230 (2000).
17. L.D. Sheng, Z. Cheng, Z. Fan, Deng Min, *Embedded EEPROM Memory Achieving Lower Power – New design of EEPROM memory for RFID tag IC*, IEEE Circuits and Devices Magazine, **22**, 6, pp. 53–59, (2006).
18. L. Mensi, L. Colalongo, A. Richelli and Z.K. Vajna, *A New Integrated Charge Pump Architecture using Dynamic Biasing of Pass Transistors*, Proceedings of ESSCIRC, Grenoble, France, 12–16 September 2005.
19. J. Che, C. Zhang, Z. Liu, Z. Wang and Z. Wang, *Ultra-Low-Voltage Low-Power Charge Pump for Solar Energy Harvesting System*, International Conference on Communications, Circuits and System (ICCCAS), California, USA, 23–25 July 2009.