In this article, power losses and total harmonic distortion performance of back-to-back converters built with 2-level topologies having different pulse width modulation schemes and 3-level topologies in a low power on-grid wind energy conversion system (WECS) have been investigated. SIMULINK/MATLAB simulation was run to calculate THD and also the determination of the switching instances of the active elements for loss calculation. A pulse by pulse calculation algorithm has been used for calculating steady state losses and switching losses. The power loss results for each topology and switching schemes have been compared. THD performances have also been compared and possible ways to decrease have also been discussed. Neutral point voltage balance of the 3-level topologies was also accomplished for more accurate and realistic results.

1. INTRODUCTION

Wind energy has become one of the world’s fastest growing energy sources due to its clean and renewable nature. Extracting the maximum power from the available wind power is of great importance in order to use available energy as efficient as possible [1, 2].

The extracted maximum available power from wind energy conversion system (WECS) is either stored in batteries or flows to the mains by means of conversion to dc or ac electrical energy with an efficient method (Fig. 1) [3].

![Fig. 1 – Back to back converter block diagram for a wind energy conversion system.](image)

The efficiency increase of an on grid WECS depends on the reduction of the power losses of the circuit elements such as semiconductors. However, the harmonic content of the current flowing to the utility grid as well as the acoustic noise induced by ac inductors have to be lowered. In this case, the switching frequency should be increased to 15 to 20 kHz range which causes increased switching losses [4].

To increase the total efficiency of the system one can implement different topologies like 2-level voltage source converters (VSC) with a special PWM method or 3-level VSC which has the inherent advantages over the former one. Studies in [5–9] state that 3-level topologies have the advantage of better voltage waveforms, lower total harmonic distortion, lower power device ratings and lower \(dV/dt\) stress. However, in 3-level topology the complexity of the system increases due to higher number of elements used. Also the neutral point voltage balance should be considered to satisfy the performance and the reliability of the system [10, 11]. In order to overcome complexity of the system, there are many studies where 2-level topology space vector pulse width modulation (SVPWM) method inherited 3-level topology SVPWM methods investigated and implemented [12–21].

On the other hand, special PWM methods like discontinuous pulse width modulation (DPWM) scheme can help to reduce the switching losses of semiconductors in a two level topology [22, 23].

The current flowing to the grid from the converter should create THD lower than 5%. The selected PWM has also a direct influence on current harmonic content [10–24].

In this study, back-to-back converters that could be used in WECS have been considered and the effects of the modulation scheme on the current harmonics and the switching losses of semiconductors have been investigated. For this purpose, MATLAB/SIMULINK program has been used to calculate current harmonics. The switching instances as well as the corresponding current values were recorded to be used as the input data for the self-made loss calculation program to calculate the steady state losses as well as the switching losses of the devices in the converters.

2. THREE-LEVEL TOPOLOGIES CONSIDERED

3-level topology was first introduced by Holtz in 1977. The very first topology has switches at its neutral point to control the voltage levels. In 1980, Nabae and his friends modified this topology such that the neutral point voltage application to the output and neutral point voltage balance have been accomplished by diode pairs [12].

These topologies have very well defined advantages over the two-level topology, one of which is being more efficient at higher switching frequencies due to the fact that the voltage level that the semiconductors see during switching is half of the total dc-link voltage. The ripple on the filter circuit is also reduced since the output voltage applied on the inductor is also half the DC-link voltage creating less THD. These two topologies are explained briefly below.

2.1. NPC TOPOLOGY

Neutral point clamped (NPC) topology where six diodes and four insulated gate bipolar transistors (IGBTs) are used to construct a half bridge (Fig. 2). The breakdown voltage class selection for the elements depends on the voltage applied on the capacitors.

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Key words: 2-level topology, 3-level topology, Space vector modulation (SVM), Power loss of semiconductors, Total harmonic distortion (THD).
When the output voltage is positive, depending on the phase current directions, the commutation will be either between outer switches or clamp diodes or between outer diodes and inner switches. As a result the turned off switches will always be clamped to the neutral point voltage which is half of the dc-link voltage allowing the use of lower blocking voltage devices compared to full dc-link voltage.

2.2. MNPC (T-TYPE NPC) TOPOLOGY

Four diodes and four IGBTs are utilized to construct a half bridge of a mixed voltage NPC (MNPC) or T-type NPC topology (Fig. 3). The output voltage levels are the same as NPC topology however the breakdown voltage selection of the switches is different. The selection method could be summarized as follows: When the output voltage is positive, depending on the load current direction, the commutation will be either between one of the half bridge switches and one of the neutral path diodes or between one of the half bridge diodes and one of the neutral path switches. As a result half bridge switches or diodes see full dc-link voltage, at blocking state. On the other hand, since the elements connected to the neutral path have one of their terminals at neutral potential, withstanding half of the dc-link voltage will be sufficient for these devices.

3. APPLYING PWM TO 2-LEVEL AND 3-LEVEL TOPOLOGIES

3.1. SPACE VECTOR PWM TECHNIQUES FOR 2-LEVEL INVERTERS

There are two widely applied pulse-width modulation (PWM) techniques: regular or natural sampled PWM method and space vector modulation (SVM) method. SVM is the preferred method over the former one due to the advantages introduced such as maximized output voltage range, minimum harmonic distortion, and even reduced switching losses [22, 23, 26–31].

The freedom to place the zero space vector to create different PWM implementations can eliminate switching instances by either allowing the outputs connected to the positive or negative dc link for duration of 1/3 switching period which allows the average switching frequency to become 2/3 of the actual switching frequency. Example: selecting switching scheme such as Discontinuous Pulse Width Modulation with 60° of nonswitching intervals – DPWM 60 (Fig. 4) which can allow centering the nonswitching instances for each phase leg symmetrically around the positive and negative peaks of its fundamental reference voltage will lead to minimized switching losses for unity power factor. It is also possible to place each 60° nonswitching period anywhere within the 120° region where the appropriate phase leg reference voltage corresponds to vicinity of the maximum/minimum of the output current such that switching losses for capacitive and inductive loads with leading and lagging power factor (PF) respectively can be minimized [23, 28–32].

3.2. APPLYING PWM TO 3-LEVEL INVERTERS

There are two main PWM techniques used for controlling 3-level topology. The first one, as in 2-level topology, is applying sinusoidal PWM by utilizing one modulating signal (sinusoidal signal) and two carrier signals or vice versa. The resulting pulses are applied to the corresponding switches. However, the drawbacks of sinusoidal signals reported in 2-level topology are also present in this PWM scheme such as low dc-link voltage usage percentage when compared with SVPWM. [12]

SVPWM used in 3-level topology has advantages like fast dynamic response and possibility to use fundamental component of the output voltage in a larger linear region. It is also possible to solve neutral point voltage balance problem. In order to apply SVPWM to a 3-level topology, three steps should be taken: finding the location of the fundamental vector in state space diagram, calculation of timings for auxiliary vectors and selecting the switching states.
In literature there have been extensive researches on SVPWM methods to make the calculation easier for control of 3-level topologies [12–21]. In order to make the calculations simpler, the researchers explored the 3-level space vector diagram by the help of 2-level space vector diagram. For this purpose, methods like allocating 2-level space vector diagram directly in the 3-level space vector diagram and finding the location of the fundamental vector inside this 2-level space vector diagram by means of using empirical equations or adapting new coordinate planes have been proposed. Once the fundamental vector is located then the auxiliary vectors are used for calculating the dwelling times. The last step is selecting the corresponding space vector states by considering the neutral point voltage balance. To some extend, the neutral point voltage is easier to balance with SVPWM due to the ability to modify redundant vector dwelling times and possibility to change switching sequence.

In a 3-level topology, depending on the switching sequence as well as the current directions, the output voltage can be at one of the three levels depicted as positive rail voltage +VDC (P), neutral point voltage V0 (O) and negative rail voltage –VDC (N). In Fig. 5, the space vector diagram also shows the possible states at which the output level can be. There are total of 27 different states as shown in Table 1. These states are named according to the vector location on the state diagram (Fig. 5).

### Table 1

<table>
<thead>
<tr>
<th>State vector description</th>
<th>State vector name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero vectors</td>
<td>PPP, OOO, NNN</td>
</tr>
<tr>
<td>Small vectors</td>
<td>POO, ONN, PPO, OON, OPP, NON, OPP, NOO, OOP, NNO, POP, ONO</td>
</tr>
<tr>
<td>Mid vectors</td>
<td>PON, OPN, NPO, NOP, ONP, PNO</td>
</tr>
<tr>
<td>Large vectors</td>
<td>PNN, PPN, NPN, NPO, NOP, ONP</td>
</tr>
</tbody>
</table>

Zero vectors and large vectors do not affect the neutral voltage balance since when zero vectors are active, current would be free wheeling and when large vectors are active; both of the capacitors C1 and C2 would be affected at the same rate without changing the neutral point voltage. However, when small and medium vectors are active, at least one of the phase currents would flow from or to the neutral point which would create neutral voltage unbalance. If the voltage unbalance is not controlled properly, the output voltage will be distorted. The voltage unbalance does also have impact on the ripple current of the capacitors affecting their life times. Depending on the severity of the unbalance, the semiconductors may also have overvoltage stress.

### 4. IMPLEMENTATION OF CONTROL STRATEGY AND SVPWM TO CONVERTER OPERATION

#### 4.1. CONTROL STRATEGY

In order to see the performance differences between 2-level converter (having been implemented with DPWM and SVPWM control) and 3-level converter (having been implemented with SVPWM control) as a result of loss performance and total harmonic distortion Matlab/Simulink simulations have been done by adopting direct current control strategy. For this purpose, two closed loop proportional integral (PI) regulators have been used to control the DC-link voltage and the AC side currents. q-axis reference signal has been produced from the dc-link voltage controller. Feed-forward decoupling values have been added to the d-q current controllers in order to form the reference \( v_d \) and \( v_q \) modulation signals (Fig. 6).

\[
\begin{align*}
    i_q^* &= \left( K_p + K_i \int dt \right) \left( V_d^* - V_{dc} \right) \\
    v_q^* &= v_q - \left( K_p + K_i \int dt \right) \left( i_q^* - i_q \right) - \omega L_i d \\
    v_d^* &= -\left( K_p + K_i \int dt \right) \left( i_d^* - i_d \right) + \omega L_i q
\end{align*}
\]

(1)

**Fig. 6 – Block diagram illustration of the controller.**

#### 4.2. IMPLEMENTATION OF SVPWM TO 3-LEVEL TOPOLOGY AND BALANCING THE NEUTRAL POINT VOLTAGE

For this study, SVPWM implementation for the 3-level inverter is managed by using 2-level space vector approach. The fundamental voltage vector location is found with the help of empirical formulas and the auxiliary vector timings are calculated. Then optimum selection of the states for minimum switching losses as well as minimum unbalance on the neutral point voltage is considered.

In order to balance the voltage, two methods are applied. First method is changing the switching sequence of the vectors so that the direction of the current to or from the neutral point will change without affecting the actual output voltage or current. The other method is modifying the dwelling time of the redundant vectors so that the duration
of the charging and discharging times of the individual dc-link capacitors will be better controlled. In order to apply these methods, the phase currents affecting the neutral point are measured and also the voltage unbalance direction is found. With these results, an algorithm that covers one or both of the appropriate methods mentioned above have been applied.

5. POWER LOSS CALCULATION OF THE TOPOLOGIES SIMULATED

Loss calculation of 2-level topologies used in hard switching inverter or converter applications is simpler when compared with 3-level topologies. The main reason is that either of the elements used in a 2-level topology have switching and conduction losses at every half period. However, in 3-level topologies, not every switch or diode have switching losses. Some of the elements may have switching losses depending on the phase angle between output voltage and the output current. In Table 2 and Table 3, switching and conduction loss distribution on the elements of MNPC and NPC topologies are shown by referencing Fig. 7. In these tables, “SW” stands for switching losses and “SS” stands for steady state losses of the elements.

![Fig. 7 - V<sub>out</sub> and I<sub>out</sub> reference figure to define SS and SW losses of the semiconductors.](image)

<table>
<thead>
<tr>
<th>Table 2</th>
<th>Distribution of loss types in a MNPC topology, x = a,b or c</th>
</tr>
</thead>
<tbody>
<tr>
<td>time</td>
<td>t&lt;sub&gt;s&lt;/sub&gt;-t&lt;sub&gt;1&lt;/sub&gt;</td>
</tr>
<tr>
<td>Magnitude</td>
<td>V&lt;sub&gt;αα&lt;/sub&gt;&lt;sup&gt;0&lt;/sup&gt;</td>
</tr>
<tr>
<td>T&lt;sub&gt;x&lt;/sub&gt;</td>
<td>0</td>
</tr>
<tr>
<td>T&lt;sub&gt;2&lt;/sub&gt;</td>
<td>0</td>
</tr>
<tr>
<td>T&lt;sub&gt;3&lt;/sub&gt;</td>
<td>SS+SW</td>
</tr>
<tr>
<td>T&lt;sub&gt;4&lt;/sub&gt;</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 3</th>
<th>Distribution of loss types in a NPC topology, x = a,b or c</th>
</tr>
</thead>
<tbody>
<tr>
<td>time</td>
<td>t&lt;sub&gt;s&lt;/sub&gt;-t&lt;sub&gt;1&lt;/sub&gt;</td>
</tr>
<tr>
<td>Magnitude</td>
<td>V&lt;sub&gt;αα&lt;/sub&gt;&lt;sup&gt;0&lt;/sup&gt;</td>
</tr>
<tr>
<td>T&lt;sub&gt;x&lt;/sub&gt;</td>
<td>0</td>
</tr>
<tr>
<td>T&lt;sub&gt;2&lt;/sub&gt;</td>
<td>0</td>
</tr>
<tr>
<td>T&lt;sub&gt;3&lt;/sub&gt;</td>
<td>SS+SW</td>
</tr>
<tr>
<td>T&lt;sub&gt;4&lt;/sub&gt;</td>
<td>0</td>
</tr>
</tbody>
</table>

By knowing the loss type of any element depending on the output phase current along with the switching instance data, a pulse by pulse calculation approach was applied. Each gate pulse of individual switches was interpreted for loss calculation if that switch or the corresponding diode has only steady state loss or both types of losses.

For the calculation of switching losses of the IGBTs and Diodes, the gate signal change of IGBTs from low to high or high to low are taken as a reference. As a result the turn-on and turn-off instances of IGBTs and recovery instances of the diodes can be found. E<sub>on</sub> (turn-on energy), E<sub>off</sub> (turn-off energy), E<sub>rr</sub> (reverse recovery energy) curves from actual IGBT and diode datasheets were recreated by implementing third order polynomial interpolation. Since the current and voltage values at each switching instances are known, with the help of E<sub>on</sub>, E<sub>off</sub>, E<sub>rr</sub> curves, the total switching losses of each element can be calculated over one period.

The steady state losses of IGBTs and diodes, on the other hand, are calculated by simply considering the IGBT gate signals being on or off. For this purpose, first of all the corresponding saturation voltage and forward voltage of the IGBTs and the diodes have been found. Polynomial interpolation was used as well for the calculation of current dependent voltage values. After having calculated the voltage values depending on the current during the on state of either the IGBT or the diode, the average steady state loss of these elements were calculated over one period.

The data used for loss calculations are taken from real IGBT and diode data of 600 V and 1200 V chips used in a Vincotech power module (10-FY12M3A040SH-M749F08). Since saturation voltage of the IGBT, forward voltage drop of the diode, E<sub>on</sub>, E<sub>off</sub> and E<sub>rr</sub> are temperature dependent, these values are considered to be at the highest junction operation temperature of 150°C which is the industrial standard at the moment.

6. COMPARISON OF SVPWM AND DPWM SIMULATION RESULTS

In 2-level back-to-back converter, one of the three phase bridges has been used as a voltage controlled current source to simulate the generator side converter whilst the other one has been used as the grid side converter which stabilizes the dc-link voltage. In 3-level back to back converter, while the three phase bridges have been used with the same purpose as their 2-level topology counterparts, the grid side converter also has an additional task which is to balance the neutral point voltage of the dc-link.

For the simulation of the systems, 9.3 kW power has been considered. The operating conditions are selected as follows: dc-link voltage: 700 Vdc, line-to-line voltage: 380 Vrms, output frequency: 50 Hz, filter inductance: 2 mH. Table 4 summarizes loss performances of 2-level and 3-level topologies as well as the THD performances. Fig. 8 and Fig. 9 illustrate the results as graphs.

When switching schemes are compared with each other in 2-level topology, SVPWM always has better THD performance over DPWM when same switching frequency values are applied to the two PWM schemes. However, if the switching frequency of SVPWM is set lower than the switching frequency of DPWM, it is possible to find switching frequency values where THD performance of
DPWM can get better than that of SVPWM while DPWM still has better overall loss performance. For instance, from Table 4, when DPWM switching frequency is selected as 16 kHz and SVPWM switching frequency is selected as 10 kHz, DPWM has better switching losses performance and THD advantage over SVPWM. As a result, even without an extra effort (building a multilevel converter or applying soft switching techniques etc), it will be possible to decrease THD and the switching losses of a system by applying DPWM when two switching schemes compared. On the other hand, the results clearly show that 3-level topologies have superior THD performance over 2-level topologies due to inherent advantages as mentioned in previous sections. When only the overall losses of 2-level and 3-level topologies are compared, total losses of 2-level topology with DPWM are comparably close to the losses of 3-level topologies.

<table>
<thead>
<tr>
<th>Topology Scheme</th>
<th>Switching frequency (kHz)</th>
<th>8</th>
<th>10</th>
<th>12.5</th>
<th>16</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-level - SVPWM</td>
<td>Total loss [W]</td>
<td>54.941</td>
<td>60.686</td>
<td>68.385</td>
<td>79.051</td>
<td>91.51</td>
</tr>
<tr>
<td></td>
<td>THD [%]</td>
<td>5.28</td>
<td>4.22</td>
<td>3.39</td>
<td>2.65</td>
<td>2.16</td>
</tr>
<tr>
<td>2-level - DPWM</td>
<td>Total loss [W]</td>
<td>42.793</td>
<td>46.062</td>
<td>49.676</td>
<td>55.603</td>
<td>61.828</td>
</tr>
<tr>
<td></td>
<td>THD [%]</td>
<td>7.79</td>
<td>6.23</td>
<td>5.26</td>
<td>4.00</td>
<td>3.37</td>
</tr>
<tr>
<td>3-level NPC - SVPWM</td>
<td>Total loss [W]</td>
<td>52.462</td>
<td>54.44</td>
<td>57.029</td>
<td>60.494</td>
<td>64.409</td>
</tr>
<tr>
<td></td>
<td>SS loss [W]</td>
<td>44.4</td>
<td>44.277</td>
<td>44.283</td>
<td>44.271</td>
<td>44.256</td>
</tr>
<tr>
<td></td>
<td>THD [%]</td>
<td>2.56</td>
<td>2.15</td>
<td>1.73</td>
<td>1.38</td>
<td>1.13</td>
</tr>
<tr>
<td>3-level MNPC - SVPWM</td>
<td>Total loss [W]</td>
<td>42.57</td>
<td>45.063</td>
<td>47.575</td>
<td>51.34</td>
<td>55.99</td>
</tr>
<tr>
<td></td>
<td>SS loss [W]</td>
<td>33.841</td>
<td>33.924</td>
<td>33.836</td>
<td>33.722</td>
<td>33.819</td>
</tr>
<tr>
<td></td>
<td>SW loss [W]</td>
<td>8.729</td>
<td>11.139</td>
<td>13.739</td>
<td>17.618</td>
<td>22.171</td>
</tr>
<tr>
<td></td>
<td>THD [%]</td>
<td>2.56</td>
<td>2.13</td>
<td>1.71</td>
<td>1.39</td>
<td>1.14</td>
</tr>
</tbody>
</table>

When loss performance of MNPC and NPC are compared with each other, the steady state loss of NPC is higher than the steady state loss of MNPC. Though 600 V devices have the advantage of lower switching losses and steady state losses when compared with 1 200 V devices, this advantage of 600 V devices does not necessarily guarantee superiority of NPC topology over MNPC topology. The fact that, when output is connected to either the positive or negative rail, current would have to pass through two 600 V devices in the NPC topology but only one 1 200 V device in the MNPC topology, gives boost to the steady state losses of NPC topology. Example: today saturation voltage of 600 V IGBT chips are in the range of 1.7 V whilst it is only in the range of 1.9 V for the 1200 V IGBTs at their rated currents.

Fig. 8 – Phase leg power loss comparison of 2-level-SVPWM, 2-level-DPWM, 3-level NPC-SVPWM, 3-level MNPC-SVPWM.

Fig. 9 – THD comparison of 2-level-SVPWM, 2-level-DPWM, 3-level NPC-SVPWM and 3-level MNPC-SVPWM.

Fig. 10 – Neutral point voltage simulation results of 3-level NPC and 3-level MNPC topologies.

Though the switching instances of elements in an MNPC topology corresponds to the switching instances of the elements in an NPC topology, the main reason of the difference between the switching losses of these two topologies is the switching energy differences due to semiconductor structure to block different voltage levels. Since 600 V devices have lower switching energies, the switching loss of NPC topology is lower.

Due to the fact that NPC and MNPC topologies have the same gate signals and the switching instances affect the neutral point voltage balance in the same direction, both of the topologies have the same neutral point balancing characteristic when the same algorithm for neutral point balancing is applied. Fig. 10 illustrates the neutral point voltage balance.

7. CONCLUSIONS

Extracting maximum power in renewable energy systems is the target for efficient use of the energy sources. However, the need for an efficient method to let the power flow to the storage devices or to the grid has also a high importance. In this study, 2-level and 3-level converter topologies along with PWM control schemes have been investigated and the module losses including steady state
and switching losses as well as the THD performances have been compared. The results have shown that, for 2-level topologies, by carefully selecting the switching frequency of DPWM higher than that of SVPWM without increasing the switching losses of DPWM beyond the switching losses of SVPWM, it is possible to find switching frequency values at which DPWM can have better THD performance. When 3-level topologies are taken into account, it was shown that not only the switching losses were lower than 2-level topologies, due to lower ripple at the output current; THD of the converter was also calculated to be lower due to inherent advantages as mentioned in previous sections. On the other hand if THD of a selected application is still in acceptable limits but is not the priority then even without an extra effort (building a multilevel converter or applying soft switching techniques etc), it will be possible to decrease overall losses of a system by applying DPWM for the sake of system simplicity.

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